

# Introduction to H-bridges

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Nov. 5, 2011

## Introduction

A circuit known as an H-bridge because of its topological resemblance to the letter, 'H', generally operates on a single voltage power supply and has the ability to apply positive or negative voltage to a load connected across the bridge. Often the bridge elements are MOSFETs which make near ideal electronic switches. Although linear variable conductance is sometimes used, the MOSFETs are generally operated digitally either ON with a resistance in the milli-ohm range or OFF with a resistance in the hundreds to thousands of meg-ohms. Pulse-width modulation (PWM) is often used to linearly vary the power to the load. A common application is to drive a DC motor at a variable speed either forwards or backwards by changing the polarity of the voltage.

## The H-bridge

A simple H-bridge is shown in Figure 1 using mechanical switches. In a real H-bridge these switches are replaced by MOSFETs. Positive voltage is applied to the load when switches 2 and 3 are ON. Negative voltage is applied to the load when switches 1 and 4 are ON. It is critical that it never be possible that switches 1 and 2 or switches 3 and 4 are ever ON at the same time. Very high current from the power source and possible destruction of the switches is possible.

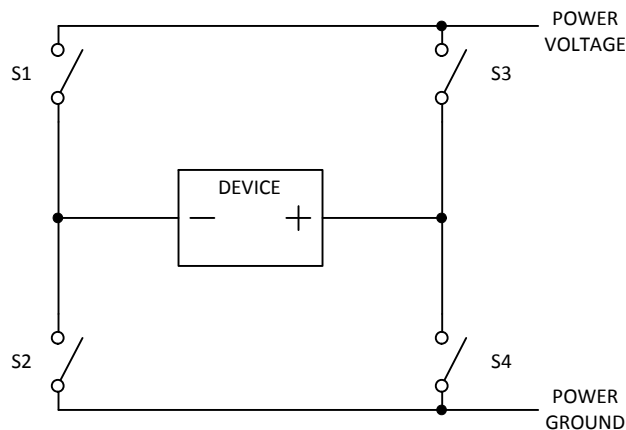


Figure 1: Basic H-bridge

In typical application, switches 1 and 3 are used to control the polarity of the voltage applied to the load and one or the other is always ON. A PWM waveform is then applied to either switch 2 or switch 4 to control the power to the load.

It should be noted that although the average voltage across the load is a linear function of the PWM duty cycle, the average voltage cannot be used in calculating power to the load for the square of the average voltage is not the same as the square of the rms voltage. However, the

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average power delivered to the load is a linear function of the PWM duty cycle. Linear control of power is a very useful feature of PWM.

## Practical implementation

A practical implementation of an H-bridge is shown in Figure 2. The circuit includes an active low ENABLE to inhibit operation while a computer is starting. A common mistake made by “newbies” is to let electronic hardware run uncontrolled while a computer is starting. Good design practice is to automatically disable hardware until the computer is ready. Also, good design practice uses a watchdog timer requiring periodic toggling by non-interrupt software. This system quickly detects a computer lockup and issues a reset to the computer and also resets all external electronics to the disable state.

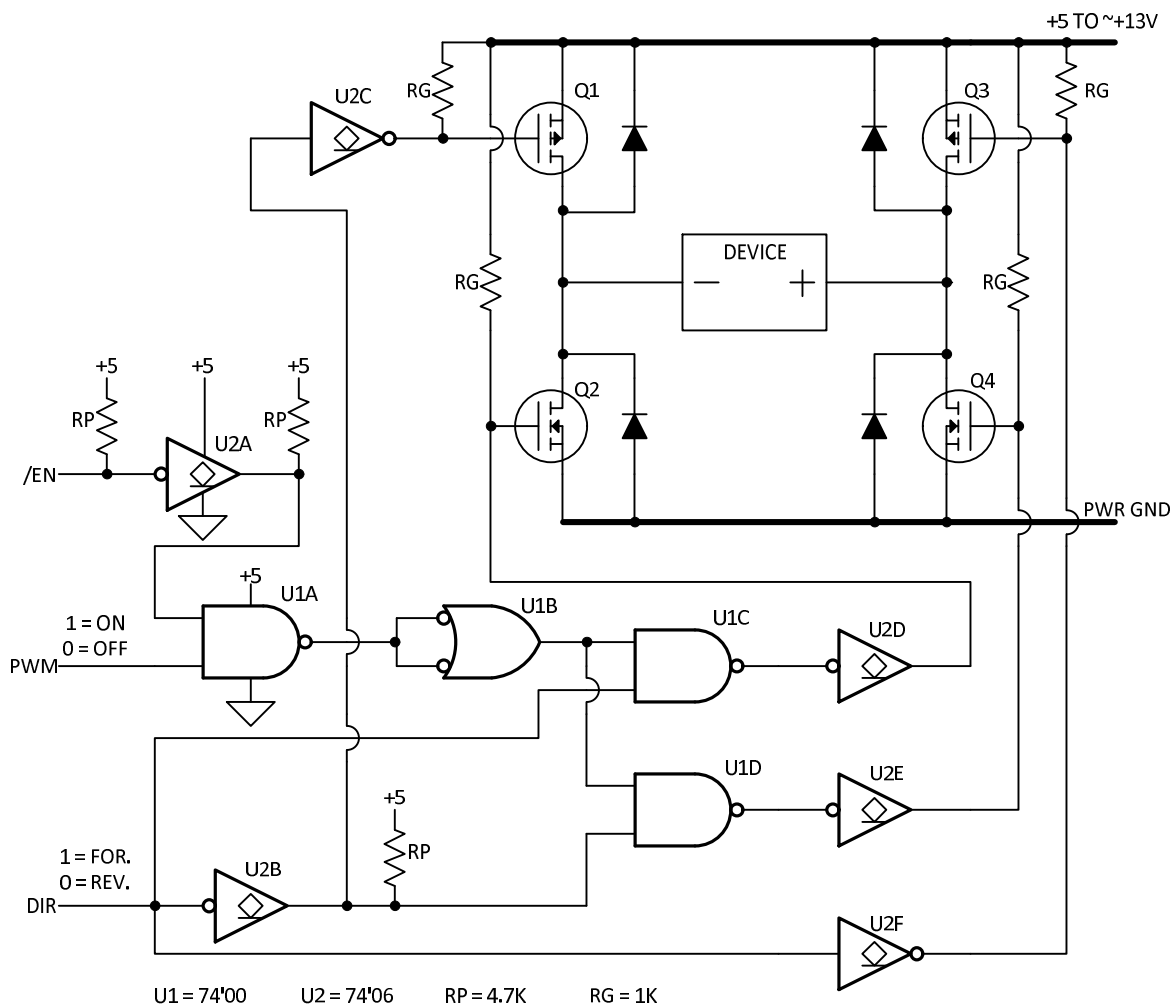


Figure 2: H-bridge implementation

The H-bridge consists of a pair of N-channel MOSFETs and a pair of P-channel MOSFETs. The DEVICE (typically a DC motor) is connected across the arms of the bridge. The logic functions are performed by a 74'00 series quad NAND gate and a 76'06 series hex high-voltage open-collector inverter. Bold lines are shown for the power to the H-bridge to indicate that these lines

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may carry high current and should go directly to the power source – preferably should be twisted to minimize loop area to reduce switching noise that can be induced into near-by electronics. The digital ground for the logic must be common with the power ground via a separate wire to the power source.

Operation for going in the forward direction is as follows. The DIRection input is at logic '1'. This makes the U2F output be at logic '0' which turns Q3 ON. The U2C output is OFF so Q1 is OFF. The PWM signal is applied to Q2 to complete the current path through the DEVICE. U1D keeps Q4 OFF.

Operation for going the reverse direction is similar to the preceding except that the DIRection input is at logic '0' which results in the U2C output being at logic '0' which turns Q1 ON and the U2F output is open which turns Q3 OFF. PWM is applied to Q4 while Q2 is OFF.

Ideally, the DIRection signal would not switch while the PWM signal is a logic '1' to prevent a possible brief moment when both Q1 and Q2 or Q3 and Q4 are ON causing a momentary high current spike. With the simple driving electronics used the switching times of the MOSFETs are probably slow enough so that this is not a problem. It is an area of uncertainty and engineers dislike uncertainty. The simple solution is probably computer software to insure the desirable state.

The pull-up resistors for the 5 volt logic are shown as 4.7K which was chosen as a convenient compromise value. Unless high speed is an issue it is rare to use less than 1K so that the logic '0' sink current does not become too high. It is also uncommon to use higher than 10K unless the specific logic family has very low input current. High resistance might slow switching times too much.

The gate resistors, RG, were chosen to be a generic 1K primarily to minimize the time constant formed by the gate-channel capacitance. Minimizing this time constant also minimizes turn-on and turn-off time of the MOSFETs. Specific designs might need a smaller resistance or could tolerate a much higher resistance. The user has to determine what is needed as there is no way for this note to be clairvoyant.

The lowest voltage that this circuit can operate with is around 5 volts unless the newer low-threshold MOSFETs are used. A 5 volt gate to channel bias is sufficient for low current loads in the low single digit ampere range – consult the data sheet before assuming the circuit will work for your application.

The highest voltage that can be used in this circuit is a function of the gate to channel breakdown voltage of the particular MOSFET. Typically this voltage is in the 14 to 18 volt range. For 24 volts the circuit would need some simple modifications –a series 1K resistor from the output of U2C and U2F to the gates Q1 and Q3 and the RG for Q2 and Q4 would be about 2K with a shunt 2K resistor to ground from the gates of Q2 and Q4. This would limit the gate-channel voltage to be 12 volts.

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The diodes across the MOSFETs conduct any back-emf from inductance in the DEVICE to prevent possible damage to the MOSFETs. These diodes should be rated for at least the maximum current the DEVICE would conduct. Ideally, these diodes would be power Schottky devices. All MOSFETS have an internal diode but it is not fast and may be ineffective for fast back-emf voltages.

### MOSFET power dissipation

The MOSFETs should be chosen with low ON resistance to minimize  $I^2R$  heating. MOSFETs can be purchased with ON resistances significantly less than 0.1 ohms (even as low as several milliohms) so for most applications requiring only a few amperes the MOSFETs will barely heat – meaning minimal or no heatsink will be needed. Note that the ON resistance specification is at high gate voltages (typically around 12 volts) relative to the source and will be somewhat higher if a low voltage for power such as 6 volts is being used. Consult the data sheet.

**Important!!! The student should do the proper engineering and compute the worst case power dissipation (occurs at 100% duty cycle) of each MOSFET (only one calculation is needed as it applies equally to all four MOSFETs). Then the student should determine what, if any, heatsink is required. For many applications no heatsink is required as the MOSFET package (typically a TO-220) can dissipate a fair fraction of a watt in free air – consult the data sheet.**