BJT Bias Design

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Introduction

Biasing is the operation of setting an operating point within an operating range. This operating point is the AC zero point and is typically offset (i.e. biased) from ground because most devices have only unipolar operation and some offset from ground is necessary to permit an AC signal to have both positive and negative swing about the operating point. The purpose of bias design is to set the collector current of a transistor to a specific value and keep deviations due to temperature and beta variations to a specified minimum. This note is the derivation of how to perform this design and covers common-base, common-emitter, and common-collector circuits. Other notes discuss how to determine proper bias conditions – a complicated process. This note is only for the design implementation of those calculations – an easy process. For this note the given values are:

- ✓ V_{CC} The main power supply voltage.
- ✓ I_C The chosen value for collector current (only for common-emitter and common-base designs)
- ✓ V_{BQ} A specified value typically for low-gain common-emitter amplifiers – if not specified then the appropriate value is determined from these notes
- ✓ V_{EQ} The target value of emitter voltage for common-collector designs only
- ✓ R_E The chosen value of R_E (only for common-collector designs)
- ✓ Tmax The maximum temperature in C that the circuit must operate in
- ✓ Tmin The minimum temperature in C that the circuit must operate in
- ✓ K_T The maximum allowable ratio of maximum to minimum collector current over the specified temperature range
- ✓ Bmax The maximum beta that the transistor might have
- ✓ Bmin The minimum beta that the transistor might have
- ✓ K_B The maximum allowable ratio of maximum to minimum collector current over the specified beta range

Design is rarely a unique calculation. There are a number of approaches to bias design which produce somewhat different results. The approach presented here is one way to achieve a good design. This particular approach has the advantage of being very methodical and not requiring any iteration. Considerable explanation is provided to assist the student in learning the design process. A key point the student should grasp is the use of ratios to simplify what would otherwise be some very complicated algebra.

Unfortunately, there are a number of design-by-rule-of-thumb procedures for biasing a transistor. These procedures may work alright for certain problems but will likely fail in others. The procedures usually do not provide you with any indication that failure is occurring so you find out the hard way after the circuit is built and tested. The procedure presented here does not depend on any rule of thumb. You have complete control over every aspect and you can follow this procedure with confidence that the result will work as specified.

This particular method is simple and ignores the effects of I_{CO} (collector to base leakage current) and Early voltage (finite collector output resistance). These are generally small effects that this course is too short to have time to consider. When I_{CO} is significant, the correct action is to reduce the ratio, (R_B/R_E). When the Early voltage is important, it will slightly alter how the collector bias voltage, V_{CQ}, is chosen.

The circuit

The circuit used for this procedure will be the simple case where a single power supply, V_{CC}, is used as shown in Figure 1. It is easy to extend this procedure to handle situations where more than one power supply voltage is used.

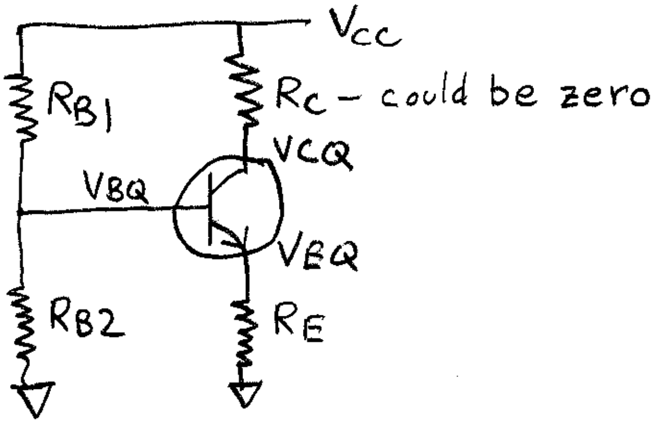

Figure 1: General circuit for BJT biasing

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Definitions:

I_C	the collector current of the transistor
I_B	the base current of the transistor
I_E	the emitter current of the transistor
V_C	the voltage between the collector of the transistor and ground
V_B	the voltage between the base of the transistor and ground
V_E	the voltage between the emitter of the transistor and ground
V_{BE}	the forward voltage across the base-emitter junction, typically around 0.65 Volts
B	the beta of the transistor
V_{BB}	the Thevenin open circuit voltage of the voltage divider, R_{B1} and R_{B2}
R_B	the Thevenin parallel resistance of R_{B1} and R_{B2}

The key analytic equation (see BJT Bias Analysis) we reverse for design is:

$$I_C = \frac{V_{BB} - V_{BE}}{R_E * (B+1)/B + R_B/B} \qquad \text{Eq. 1}$$

Design for temperature stability

The first step in bias design is establishing the temperature stability of the collector current. At typical operating currents, V_{BE} has a temperature coefficient of about -0.0022 Volts per degree C. It will be higher or lower than this depending on the collector current but there is not time to consider this in this course. The typical value provides very good results. Thus, if the temperature of the environment the transistor is operating in increases 10 degrees C, then V_{BE} will drop by 0.022 Volts. This in turn will cause the collector current to increase and the collector voltage to drop (assuming R_C is not 0). The maximum collector current, $I_C$max, occurs at the maximum operating temperature. The minimum collector current, $I_C$min, occurs at the minimum operating temperature. With the appropriate choice of V_{BB}, the variation in collector current can be held to within acceptable limits. The minimum and maximum temperature that the transistor amplifier will operate in must be specified or established.

Tmin	the minimum operating temperature in degrees C
Tmax	the maximum operating temperature in degrees C

You may either be given this information or (more likely) you may have to determine it yourself. The following table provides some rough guidelines to assist you in choosing a Tmin and Tmax if they are not specified to you.

Tmin	Tmax	Environment
10	40	if the amplifier will operate only in an environment occupied by people
0	50	if the amplifier will operate indoors only
-40	65	if the amplifier will operate outdoors or in extreme temperature conditions
-55	125	an extreme case sometimes used for military electronics design

The next step is to determine the maximum and minimum V_{BE} values at the temperature extremes. This requires that you know what V_{BE} is nominally at 25 degrees C – this is often available from the data sheet. This value is a function of the emitter current but is typically around 0.65 Volts. Use this value for V_{BE25} until you have better information.

$$V_{BE}\text{min} = V_{BE25} - (\text{Tmax} - 25) * 0.0022 \qquad \text{Eq. 2}$$

$$V_{BE}\text{max} = V_{BE25} + (25 - \text{Tmin}) * 0.0022 \qquad \text{Eq. 3}$$

The goal of bias stability design is to keep the collector current constant within an acceptable factor over the entire specified temperature range. In many designs, +-10 percent variation is tolerable. In some cases the variation must be limited to +-5 percent. In other cases a +-20 percent variation can be tolerated. An alternate way to express this that is very convenient for our use is to specify the ratio of $I_C\text{max} / I_C\text{min}$. We call this ratio K_T because it is a specified constant pertaining to temperature stability.

$$K_T = I_C\text{max} / I_C\text{min} \qquad \text{Eq. 4}$$

Note that a collector current variation of +-5 percent would correspond to a K_T of about 1.1, a +-10 percent variation would correspond to a K_T of about 1.2, and a variation of +-20 percent would correspond to a K_T of 1.5. In addition to being told or determining the operating temperature range, you must also either be told or determine for yourself an appropriate value for K_T. For most cases a K_T value of 1.2 is adequate unless there is a reason to use something different.

Now we are ready to solve Equation 1 for the minimum V_{BB} that will give us the required collector current stability with temperature. For this problem, the denominator of Equation 1 will not be changing so it will be referred to as denominator. We can now write:

$$K_T = \frac{I_C\text{max}}{I_C\text{min}} = \frac{(V_{BB} - V_{BE}\text{min}) / \text{denominator}}{(V_{BB} - V_{BE}\text{max}) / \text{denominator}} = \frac{V_{BB} - V_{BE}\text{min}}{V_{BB} - V_{BE}\text{max}} \qquad \text{Eq. 5}$$

The only unknown is V_{BB}. The reason for expressing K_T as a ratio is now obvious. We solve for V_{BB} noting that this is the minimum value that will meet the K_T specification. We can always use a higher value and frequently will in common-collector designs. Solving Equation 5 for the minimum value of V_{BB} to use gives:

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$$\mathbf{V_{BB}min = \frac{K_T * V_{BE}max - V_{BE}min}{K_T - 1}} \qquad \textbf{Eq. 6}$$

Now you may either choose $V_{BB} = V_{BB}$min or round up the calculation to a higher value. At any rate, you now have a value for V_{BB}.

The average value of V_{BE} over the given temperature range will be used in subsequent calculations and is calculated by Equation 7.

$$\mathbf{V_{BE}nom = (V_{BE}min + V_{BE}max) / 2} \qquad \textbf{Eq. 7}$$

Design for beta stability

One fact of life we have to live with is that the beta of one transistor compared to another of the same type may vary over a wide range (80 to 240 would be typical). It is desirable for the bias design to be such that the collector current is the target value plus or minus a small percentage regardless of what the beta actually is. Unlike the issue of temperature stability, beta is not varying (at least very much) in a particular transistor. But the beta of individual transistors in a production run of the circuit can be expected to vary considerably. All the circuits should work the same regardless of beta.

The design solution will be to form a ratio involving Equation 1 such that we can solve for a ratio of the maximum to minimum collector current. This time the numerator of the equation will not matter so it will be referred to as numerator. We will call this ratio K_B because it is a specified constant pertaining to stability with beta. K_B will be a specified value just like K_T was for temperature stability. The nominal choice for K_B will be 1.2 unless there is a reason to choose a different value. Looking at Equation 1 it is observed that the maximum collector current would occur at the highest beta and the minimum collector current would occur at the lowest beta. So, knowing Bmax and Bmin for a particular transistor type, we can write:

$$K_B = \frac{I_C\text{max}}{I_C\text{min}} = \frac{\dfrac{\text{numerator}}{R_E * (\text{Bmax} + 1)/\text{Bmax} + R_B/\text{Bmax}}}{\dfrac{\text{numerator}}{R_E * (\text{Bmin} + 1)/\text{Bmin} + R_B/\text{Bmin}}} \qquad \text{Eq. 8}$$

The numerator terms will cancel. At this point, K_B, Bmax, and Bmin are known. We do not yet know R_B or R_E. With this one equation we can not solve for either. But we can solve for the ratio of the two. Equation 8 is now modified to make (R_B/R_E) a single variable.

$$K_B = \frac{(Bmin + 1)/Bmin + (R_B/R_E)/Bmin}{(Bmax + 1)/Bmax + (R_B/R_E)/Bmax} \qquad \text{Eq. 9}$$

Now it is possible to solve for the quantity (R_B/R_E) even though we do not yet know the individual values – this is why ratios are so useful. What we are actually solving for is the maximum ratio that will meet the given K_B specification. We can always use a smaller ratio in an actual design. However, in common-emitter and common-collector designs, R_B is in parallel with the input and we generally want to maximize R_B so that it does not make the input impedance of the amplifier any lower than necessary. So, we will calculate the maximum and then use that value in subsequent calculations. Solving Equation 9 for (R_B/R_E) gives:

$$\mathbf{(R_B/R_E)max = \frac{K_B * (Bmax + 1)/Bmax - (Bmin + 1)/Bmin}{(1/Bmin) - (K_B/Bmax)}} \qquad \textbf{Eq. 10}$$

Since beta can vary over a wide range, the geometric mean of beta will be used in subsequent calculations as given by Equation 11.

Bnom = sqrt(Bmin * Bmax) **Eq. 11**

Special biasing for common-collector amplifiers

The collector resistor, R_C, is normally zero in common-collector amplifiers. Any value that might exist does not affect biasing. Given the specified V_{EQ} and R_E, then I_E is calculated as:

$$I_E = V_{EQ} / R_E \qquad \text{Eq. 12}$$

Then, I_B is calculated as:

$$I_B = I_E/(B+1) = V_{EQ}/((B+1) * R_E) \qquad \text{Eq. 13}$$

Then, R_B is calculated as:

$$R_B = R_E * (R_B/R_E) \qquad \text{Eq. 14}$$

The voltage drop across R_B is then:

$$\begin{aligned} V_{RB} &= I_B * R_B = V_{EQ}/((B+1) * R_E) * R_E * (R_B/R_E) \\ &= V_{EQ} * (R_B/R_E) / (B+1) \qquad \text{Eq. 15} \end{aligned}$$

Now, using Kirchoff's voltage law, we can calculate the required value of V_{BB}. This value generally supersedes the calculation performed previously for temperature stability as this result is usually significantly larger thus providing very good temperature stability. However, we would use the larger of the two results.

$$\mathbf{V_{BB} = V_{EQ} + V_{BE}nom + V_{EQ} * (R_B/R_E)/(B+1)} \qquad \textbf{Eq. 16}$$

Finally, the collector current is:

$$I_C = (B/B+1) * V_{EQ}/R_E \qquad \text{Eq. 17}$$

Use the specified value of R_E and calculated value for V_{BB} in this section and the maximum value for $(R_B/_{RE})$ as determined previously and go to the section below on calculating R_{B1} and R_{B2}.

Special biasing for common-base and common-emitter amplifiers

For this case the collector current, I_C, is either specified or determined from Equation 18 if V_{CQ} and R_C are known.

$$I_C = (V_{CC} - V_{CQ}) / R_C \qquad \text{Eq. 18}$$

At this point, I_C is now known. We now proceed to calculating R_E.

All of the previous steps now come together to enable us to calculate R_E. For this calculation, we will factor R_E out of Equation 1:

$$I_C = \frac{V_{BB} - V_{BE}nom}{[(Bnom + 1)/Bnom + (R_B/R_E)/Bnom] * R_E} \qquad \text{Eq. 19}$$

Equation 19 is a modified form of Equation 1 that has the quantity, (R_B/R_E). Solving Equation 19 for RE gives:

$$\mathbf{R_E = \frac{V_{BB} - V_{BE}nom}{[(Bnom + 1)/Bnom + (R_B/R_E)/Bnom] * I_C}} \qquad \textbf{Eq. 20}$$

The calculation for R_E is not likely to produce a standard resistor value. So, we will round the calculated value of R_E to the nearest standard value and use this standard value in the subsequent calculations for R_B to minimize accumulative errors.

For low-gain amplifiers V_{BQ} may be specified (from complicated calculations in another note) to optimize the linear dynamic range. If so then this value is typically significantly higher than the V_{BB}min determined previously for temperature stability. Thus, a specified V_{BQ} supersedes that calculation. If V_{BQ} was specified then determine V_{BB} from Equation 21. The student should derive this equation – it comes from the analytical equation derived in the note for bias analysis but has been inverted and equivalent terms for I_B and R_B have been substituted.

$$\mathbf{V_{BB} = V_{BQ} + (I_C / Bnom) * R_E * (R_B/R_E)} \qquad \textbf{Eq. 21}$$

Use the chosen value for R_E, the appropriate value for V_{BB}, and the maximum value for (R_B/R_E) as determined previously and go to the section below on calculating R_{B1} and R_{B2}.

Calculating R_{B1} and R_{B2}

First, we calculate R_B by multiplying the standard value chosen for R_E by the ratio (R_B/R_E).

$$R_B = R_E * (R_B/R_E) \qquad \text{Eq. 22}$$

We do <u>not</u> round this value. Our goal now is to determine a voltage divider composed of R_{B1} and R_{B2} such that we obtain the V_{BB} determined earlier and R_B as just determined.

The voltage division to obtain V_{BB} is:

$$V_{BB} = V_{CC} * R_{B2} / (R_{B1} + R_{B2}) = V_{CC} / [(R_{B1}/R_{B2}) + 1] \qquad \text{Eq. 23}$$

Knowing V_{BB} from earlier calculations and knowing V_{CC}, we can solve for (R_{B1}/R_{B2}) even though we do not yet know the individual values.

$$\mathbf{(R_{B1}/R_{B2}) = (V_{CC}/V_{BB}) - 1} \qquad \textbf{Eq. 24}$$

We know that RB is the parallel combination of R_{B1} and R_{B2}. So, we can write:

$$R_B = \frac{R_{B1} * R_{B2}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{(R_{B1}/R_{B2}) + 1} \qquad \text{Eq. 25}$$

Equation 25 is then simply solved for R_{B1}.

$$R_{B1} = R_B * [(R_{B1}/R_{B2}) + 1] \qquad \text{Eq. 26}$$

If we factor in Equation 24, then we can express Equation 26 as:

$$\mathbf{R_{B1} = R_B * (V_{CC}/V_{BB})} \qquad \textbf{Eq. 27}$$

The calculated value for R_{B1} is not likely to be a standard resistor value. So, we will round the calculated value to the nearest standard value and proceed. R_{B2} will be based on this rounded value rather than the original calculated value to minimize error accumulation.

Since we now know R_{B1} and the quantity (R_{B1}/R_{B2}), then we can calculate the value of R_{B2} using the just determined standard resistor value for R_{B1}:

$$\mathbf{R_{B2} = R_{B1} / (R_{B1}/R_{B2})} \qquad \textbf{Eq. 28}$$

Again, we will round the calculated value of R_{B2} to the nearest standard resistor value.

The bias design is now complete. The last step in any design is checking or verification. Analyze your design to see if it produces the required collector current.

It is left as an exercise for the student to produce their own summary of the information in this note for use in solving design problems on tests.