Common-Collector Amplifier Design

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Introduction

This note describes the process for designing a common-collector amplifier. Common-collector amplifiers have two applications. The first is at the input of an amplifier chain to raise the input impedance. The second is at the output of an amplifier chain to lower the output resistance. In the design of a common-collector amplifier there is a tradeoff between power gain and output signal swing. A common-collector amplifier at the input of an amplifier chain would likely be designed to maximize the power gain since the output signal is going to be too small for signal swing to be an issue. A common-collector amplifier at the output of an amplifier chain driving the load resistance would likely be designed for maximum signal swing at the forfeit of power gain. The choice of emitter resistor, R_E, and the bias point, V_{EQ}, vary depending on whether power gain or signal swing is important. Both will be discussed in detail.

Choice of emitter resistor, R_E

The design of a common-collector amplifier begins with the choice of R_E based on knowing the load resistance, R_L. Rather than discuss specific ohmic values for R_E and R_L, it is simpler to discuss the generic ratio, (R_E/R_L), since that is the only real variable. The power gain of the amplifier is made large by making this ratio large. The linear output signal swing is made large by making this ratio small. Thus, a tradeoff has to be made. There are two competing mathematics here – one for power gain and the other for linear output signal swing. Both of these mathematics will be developed below.

Mathematics for power gain

For practical reasons this discussion will assume that the dynamic emitter resistance, re, is small in comparison to the parallel combination of R_E and R_L, $R_E||R_L$, and can thus be ignored. This is a good approximation for any well designed common-collector amplifier and lets us ignore what generally ends up being small variations in the calculations based on bias voltage and currents. The error in doing this is in the direction of making the computed power gain a bit larger than it will actually be. The goal here is to understand how to make the power gain high rather than to calculate the exact value.

The input resistance of the amplifier is the base bias resistance, R_B, in parallel with $(B+1)*(R_E||R_L)$ remembering that we are ignoring the small effect of re and noting that B is the beta of the transistor. In the design for bias stability with beta we know that the ratio, (R_B/R_E) will be a certain maximum value, $(R_B/R_E)max$, based on the collector current stability requirements and the spread of beta for the transistor. In general, we use the maximum value since that maximizes R_B and thus the input resistance of the

amplifier. Maximizing the input resistance helps to maximize the power gain. We can now develop the equation for the input resistance of the amplifier.

$$Rin = R_B \,||\, [(B+1) * (R_E||R_L)]$$

$$= \frac{(R_B/R_E)max * (B+1) * R_E * R_L}{(R_B/R_E)max + (B+1) * R_E * R_L) * \frac{(R_E + R_L)}{R_E + R_L}}$$

$$= \frac{(R_B/R_E)max * (B+1) * R_E * R_L}{(R_B/R_E)max * (R_E + R_L) + (B+1) * R_L}$$

$$= \frac{(R_B/R_E)max * (B+1) * R_E}{(R_B/R_E)max * [(R_E/R_L) + 1] + (B+1)}$$

$$Rin = \frac{(R_B/R_E)max * (R_E/R_L) * R_L}{[(R_B/R_E)max / (B+1)] * ((R_E/R_L) + 1) + 1} \qquad \text{Eq. 1}$$

Ignoring the effect of re we will take the output signal voltage of the amplifier to be equal to the input signal voltage for a voltage gain, Av, of 1.0. Typically the gain might be between around 0.9 and 0.98 so this is not a bad approximation. The equation for power gain, pg, is:

$$pg = \frac{Poutput}{Pinput} = \frac{(Av * Vin)^2 / R_L}{Vin^2 / Rin} \qquad \text{Eq. 2}$$

Since we are taking the voltage gain to be 1.0 then Equation 2 simplifies to:

$$pg = \frac{Rin}{R_L} \qquad \text{Eq. 3}$$

Substituting Equation 1 into Equation 3 and simplifying gives:

$$pg = \frac{(R_B/R_E)max * (R_E/R_L)}{[(R_B/R_E)max / (B+1)] * ((R_E/R_L) + 1) + 1} \qquad \text{Eq. 4}$$

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In round numbers, a typical value for (R_B/R_E)max is in the 13 to 25 range and a typical value for B is 100. Figure 1 is a plot of substituting these typical values into Equation 4 and plotting the power gain versus (R_E/R_L).

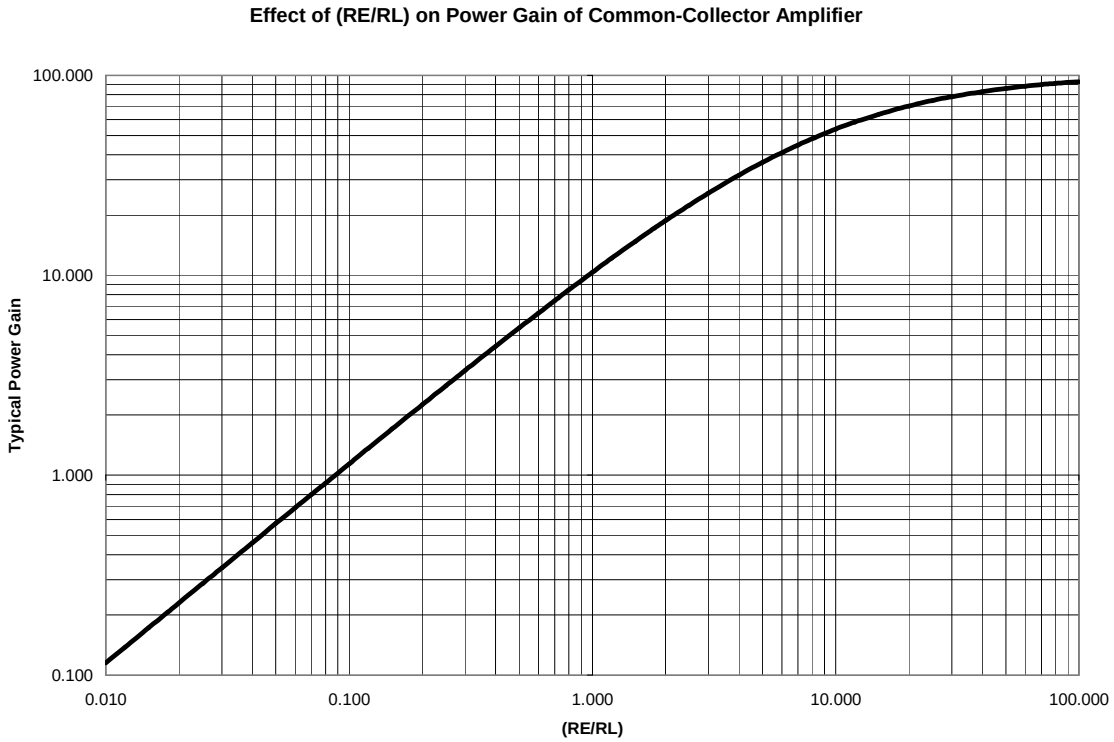

Figure 1: Typical power gain versus (R_E/R_L)

Observing Figure 1 it can be noted that the amplifier is useless for (R_E/R_L) less than 0.1 as the power gain becomes less than 1.0. It can also be observed that the ultimate power gain possible approaches 100 as (R_E/R_L) is made very large.

Mathematics for maximum output signal swing

For simplicity we will assume that the output signal is a sine wave with a peak voltage, Vp. It really does not matter what the wave shape is but a sine wave is easy to discuss. The general idea is for the emitter current to vary from zero to twice the quiescent emitter current, I_{EQ}, at the maximum output signal swing. What value of quiescent emitter voltage, V_{EQ}, maximizes the output signal swing? If V_{EQ} is too low then the maximum output is limited because the emitter current can not be less than zero. If V_{EQ} is too high then the maximum output is limited because the emitter voltage can not be higher than the power supply voltage, V_{CC}.

First we develop an equation that determines the peak output voltage possible for a given V_{EQ}. We start at the point where the emitter current is zero. Note that when the emitter current is zero that the emitter voltage is greater than zero because of discharge of the

coupling capacitor. The coupling capacitor to the load is charged to V_{EQ} but this charge increases and decreases slightly with the signal assuming the time constant is long compared to the signal frequency. Thus, at the optimum bias point and with the maximum possible output signal swing we have the case that the emitter current is zero but the current through R_E is greater than zero at the negative peak of the signal. This is illustrated in Figure 2.

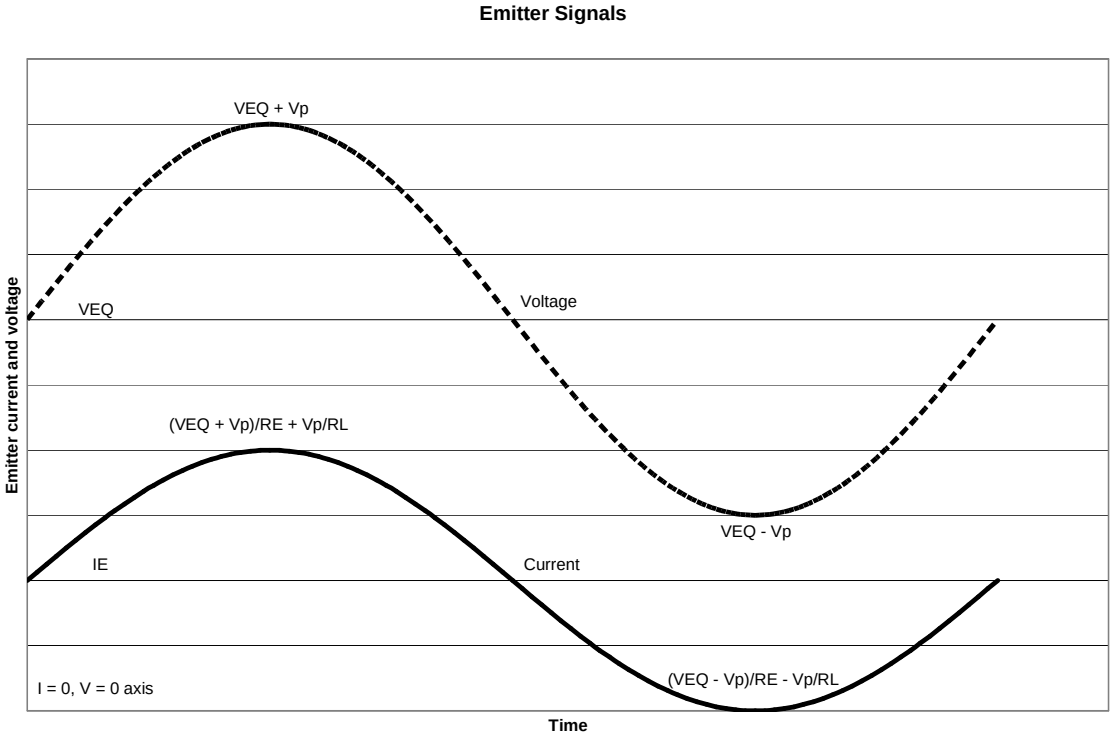

Figure 2: Emitter current and voltage signals

The emitter current, I_E, is:

$$I_E = \frac{V_{EQ}}{R_E} + \frac{V_O}{R_E} + \frac{V_O}{R_L} = \frac{V_{EQ} + V_O}{R_E} + \frac{V_O}{R_L} \qquad \text{Eq. 5}$$

When V_O is at the negative peak, -Vp, then the emitter current is:

$$I_E = \frac{V_{EQ} - Vp}{R_E} - \frac{Vp}{R_L} = 0 \qquad \text{Eq. 6}$$

Solving for 0 gives:

$$\frac{V_{EQ} - Vp}{R_E} = \frac{Vp}{R_L} \qquad \text{Eq. 7}$$

which can be written as:

$$V_{EQ} - Vp = Vp * (R_E/R_L) \qquad \text{Eq. 8}$$

For simplicity in the following development we define:

$$\mathbf{K = (R_E/R_L)} \qquad \mathbf{Eq. 9}$$

Solving Equation 7 for V_{EQ} gives:

$$\mathbf{V_{EQ} = (1 + K) * Vp} \qquad \mathbf{Eq. 10}$$

Solving Equation 10 for Vp gives:

$$\mathbf{Vp = V_{EQ} / (1 + K)} \qquad \mathbf{Eq. 11}$$

Note that the minimum emitter voltage, $V_E$min is:

$$V_E\text{min} = V_{EQ} - Vp$$

$$= V_{EQ} - V_{EQ} / (1 + K)$$

$$V_E\text{min} = K * V_{EQ} / (1 + K) \qquad \text{Eq. 12}$$

The maximum possible emitter voltage, $V_E$max, is equal to V_{CC} minus the collector-emitter saturation voltage, V_{CE}sat, which is typically several tenths of a volt at low milliampere currents. Expressed as an equation gives:

$$V_E\text{max} = V_{CC} - V_{CE}\text{sat} \qquad \text{Eq. 13}$$

Now we can solve for the optimum V_{EQ} that maximizes large signal swing. The maximum possible linear output signal swing is:

$$V_O\text{ppmax} = 2 * Vp = V_E\text{max} - V_E\text{min}$$

$$= [V_{CC} - V_{CE}\text{sat}] - [K * V_{EQ} / (1 + K)]$$

$$= [V_{CC} - V_{CE}\text{sat}] - [K * (1 + K) * Vp / (1 + K)]$$

$$= [V_{CC} - V_{CE}\text{sat}] - [K * Vp]$$

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$V_O ppmax = [V_{CC} - V_{CE}sat] - [K * V_O ppmax / 2]$ Eq. 14

Solving Equation 14 for $V_O ppmax$ gives:

$V_O ppmax = [V_{CC} - V_{CE}sat] / (1 + K/2)$ **Eq. 15**

Remember that this is the maximum possible linear output signal swing. We can substitute this value into Equation 11 to determine the corresponding optimum V_{EQ}.

$V_O ppmax = 2 * Vp = 2 * V_{EQ} / (1 + K) = (V_{CC} - V_{CE}sat) / (1 + K/2)$ Eq. 16

$$V_{EQ}opt = \frac{(V_{CC} - V_{CE}sat)}{1 + K/2} * \frac{1 + K}{2}$$ Eq. 17

Equation 17 simplifies to:

$V_{EQ}opt = (V_{CC} - V_{CE}sat) * (1 + K) / (2 + K)$ **Eq. 18**

Equation 18 is our solution and tells us the optimum quiescent emitter voltage to bias the transistor to achieve the maximum possible linear signal swing for a given choice of (R_E/R_L).

Effects of the choice of K (R_E/R_L)

The normalized power gain is found by substituting the typical values for $(R_B/R_E)max$ and B into Equation 4 and the diving the result by the ultimate power gain when (R_E/R_L) approaches infinity. Thus the normalized maximum power gain is 1.0.

The normalized maximum possible output signal swing is found by dividing Equation 15 by $(V_{CC} - V_{CE}sat)$. Thus, the normalized maximum output signal swing is 1.0.

The "Goodness of Choice" curve is the product of the normalized power gain and normalized maximum output signal swing curves scaled so that the maximum is 1.0.

Figure 3 shows the three normalized curves as a function of (R_E/R_L). The peak of the "Goodness of Choice" curve occurs at an (R_E/R_L) of just over 4 but not too much should be read into this as the applications for a common-collector amplifier are widely separated. The maximum power gain for use as a high impedance input stage occurs when (R_E/R_L) is in the range of 10 to 40. Higher values only produce a small improvement in gain. The maximum possible output signal swing for use as a low impedance output stage occurs when (R_E/R_L) is in the range of 0.5 to 1.0. Smaller values only produce slightly more signal swing at the expense of a power gain that is approaching 1.0.

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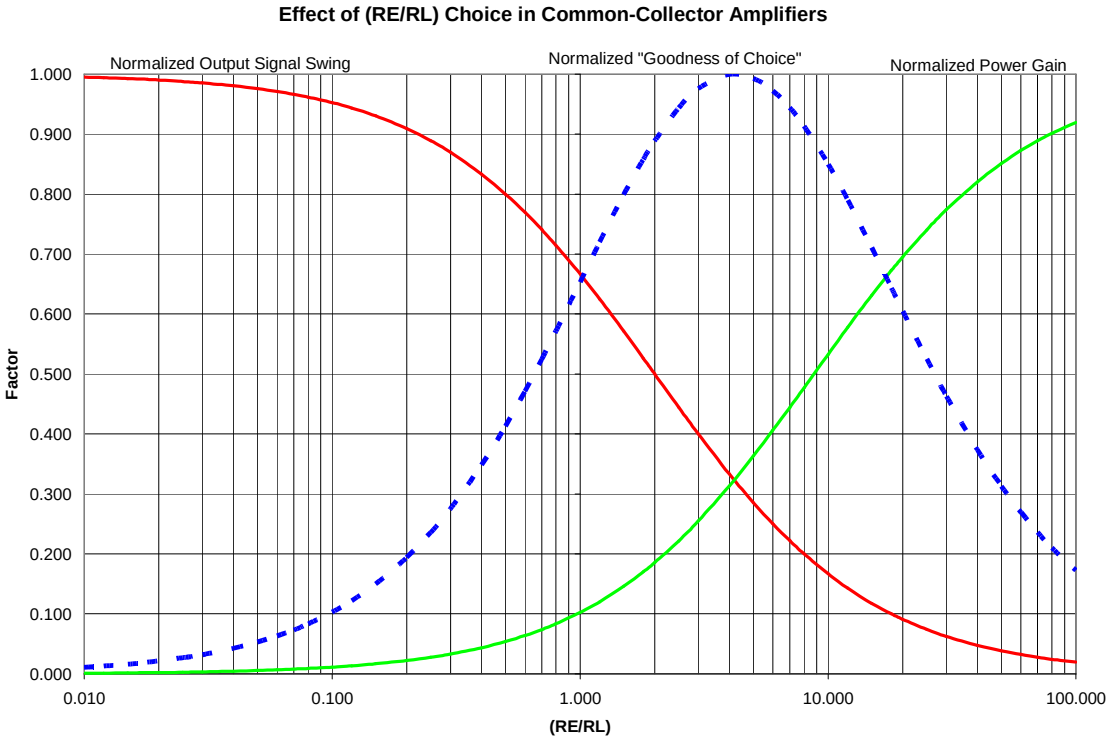

Figure 3: Effects of the choice of (R_E/R_L)

Optimum V_{EQ} as a function of (R_E/R_L)

Using the simplifying assumption that VCEsat is negligibly small as compared to V_{CC}, Figure 4 shows the ratio of optimum V_{EQ} to V_{CC} for a given K = (R_E/R_L). For low values of K that would be used in an output stage design the signal swing is large and the optimum V_{EQ} approaches one-half V_{CC}. For higher values of K that would be used in an input stage design in order obtain higher power gain the optimum V_{EQ} / V_{CC} ratio approaches V_{CC}. Real values will not approach V_{CC} as close as shown in this plot – see the next section on input stage design for other practical considerations.

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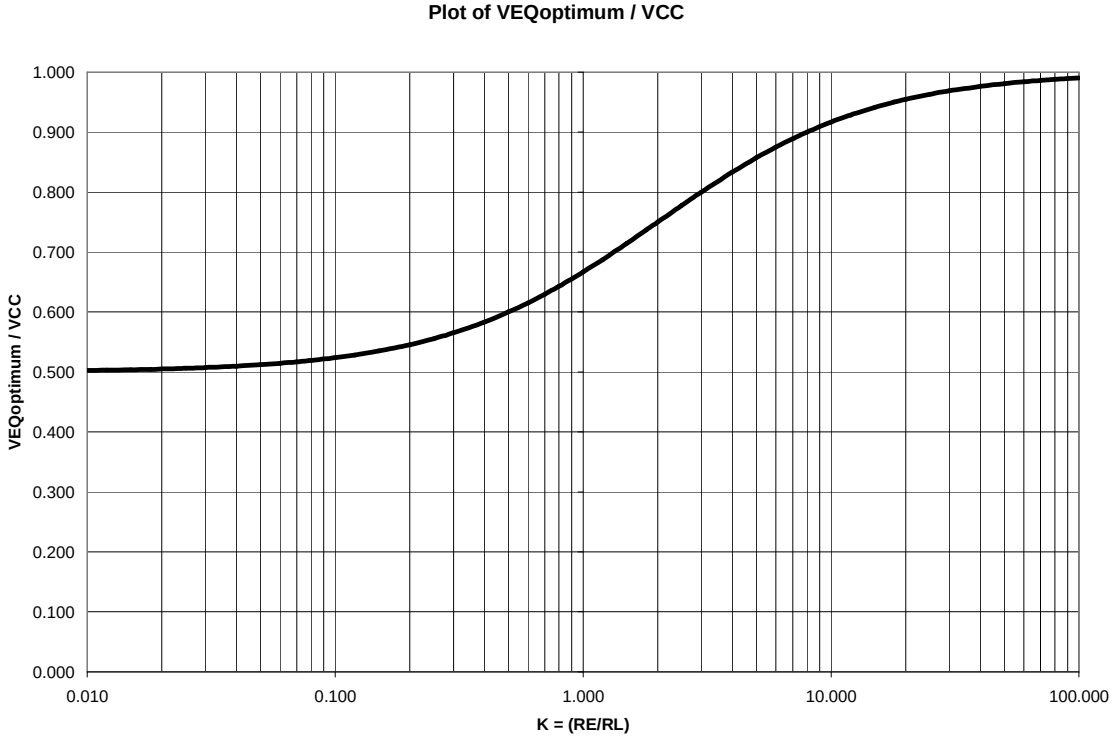

Figure 4: Optimum V_{EQ}/V_{CC} versus R_E/R_L

Input stage design

When the common-collector amplifier is used as an input stage the signal amplitude is generally very small and signal swing is not a concern. The design focuses on obtaining the maximum practical power gain instead. For this case we use the highest V_{EQ} consistent with a linear output signal swing of the largest input signal of interest. This allows us to use a relatively high value of R_E which leads to a corresponding increase in R_B thus raising the input resistance of the amplifier which achieves the goal of increasing the power gain. The maximum input signal of interest may be millivolts or less or perhaps as large as several tenths of a volt peak to peak. For the transistor to operate with the best characteristics the minimum voltage from the collector to the emitter, V_{CE}min, should be at least around a volt – preferably greater. This is a higher voltage than the V_{CE}sat used in the previous large signal calculations. This higher voltage is necessary because V_{BB} and the corresponding V_{BQ} must end up as values less than V_{CC} by at least several tenths of a volt. Using the large signal algebra for this case could result in a V_{BB} or V_{BQ} greater than V_{CC} which will not work. The difference is that in the large signal case, V_{EQ} was significantly below V_{CC} whereas in the small signal case V_{EQ} is close to V_{CC}. The design procedure is as follows. This procedure assumes that the input signal is relatively small. No test is done to determine if the input signal is too high (i.e. many volts peak to peak) for this design procedure to produce linear output. If the input signal is high then it may be better to use the output stage design procedure.

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Step 1: Specify V_{IN}ppmax (if less than 0.1 volts then use 0.1 volts).

Step 2: Specify V_{CC} and V_{CE}min. The higher V_{CC} is the more room there is to make V_{CE}min larger. Equation 20 gives good results for V_{CC} greater than about 3 volts.

$$V_{CE}\text{min} = 1 + V_{CC} / 10 \qquad \text{Eq. 20}$$

Step 3: Calculate the highest possible V_{EQ} and use that value. Note that the positive peak of the maximum output signal just touches the level defined by V_{CC}- V_{CE}min. That is as high as we want to operate. The transistor will actually work with less voltage across it so we have some ill defined margin here. Note that the purpose of the factor is to lower V_{EQ} just a bit so that we have a well defined margin.

$$V_{EQ}\text{max} = V_{CC} - V_{CE}\text{min} - (V_{IN}\text{ppmax} * \text{factor})/2 \qquad \text{Eq. 21}$$

where factor is 1.0 for large signals and up to about 3.0 for small signals.

Step 4: Calculate the maximum value of (R_E/R_L) consistent with linear signal swing by solving Equation 11 in reverse for Kmax. Note that Vp has been replaced by V_{IN}ppmax / 2. V_{EQ} is the maximum as calculated in step 3.

$$(R_E/R_L)\text{max} = \frac{V_{EQ}}{(V_{IN}\text{ppmax} / 2)} - 1 \qquad \text{Eq. 22}$$

Step 5: Given R_L, then calculate $R_E = (R_E/R_L)\text{max} * R_L$ and round down to the nearest standard resistor value.

Step 6: Using the specified beta stability factor, K_B, and the specified range of beta, calculate (R_B/R_E)max and then use this value to complete the determination of R_{B1} and R_{B2} using the standard bias design method.

Output stage design

In the design of a common-collector output stage the goal is to deliver a high amplitude linear signal to the load. There is an optimum value for V_{EQ} and we are driven to make (R_E/R_L) as small as practical because that increases the emitter current of the transistor thus increasing the maximum linear output voltage swing. However, we must not make (R_E/R_L) too small because the resulting low input resistance the amplifier will have may cause significant voltage division from the signal source thus lowering the maximum output amplitude. The idea is to make (R_E/R_L) only as small as required to do the job.

Step 1: Specify V_{CC}, V_{CE}sat, and V_{IN}ppmax. For small signal amplifiers a value of V_{CE}sat of 0.5 volts is more than adequate.

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Step 2: Use Equation 15 in reverse and let $V_O$ppmax equal V_{IN}ppmax to calculate a maximum value of K or (R_E/R_L). Be wary of a value of K less than 0.5 as the power gain of the amplifier is quickly approaching 1. It not recommended to use a value less than 0.5 for K unless absolutely necessary. A value of 1 is more reasonable although the maximum output signal swing is somewhat more limited.

$$K_{max} = 2 * \left(\frac{V_{CC} - V_{CE}sat}{V_{IN}ppmax} - 1 \right) \qquad \text{Eq. 22}$$

Step 4: Given R_L, calculate $R_E = K_{max} * R_L$ and round down to the nearest standard resistor value.

Step 5: Using the specified beta stability factor, K_B, and the specified range of beta, calculate $(R_B/R_E)_{max}$ and then use this value to complete the determination of R_{B1} and R_{B2} using the standard bias design method.

Preliminary test prior to completing either input or output stage design

The first issue we must address is to confirm that a common-collector amplifier is appropriate. It does no good to design a nice common-collector amplifier for a situation for which it will be worse than nothing. A common-collector amplifier transforms a signal at a relatively high impedance into a slightly less signal at a relatively low impedance. That is the mechanism for power gain. The load resistance must be less than the input resistance of the amplifier in order for the net power gain to be greater than 1.0. In the case of the amplifier used as an output stage, the input resistance of the amplifier should be at least twice the output resistance of the previous stage so that voltage division at the input does not significantly reduce the signal level.

Figure 5 shows a typical value of input resistance as the emitter resistance is varied. The plot is shown in normalized form to be more general. The conclusions from the plot are that for an input stage that R_E should be large in comparison to R_L so that the input resistance can be high. The plot also illustrates that when R_E is small compared to R_L as would typically be the case for an output stage that the corresponding input resistance is low.

Figure 6 assists in the choice of R_E/R_L for a given R_S/R_L and a desired R_{in}/R_S to minimize the input voltage division. It is generally desirable for R_{in}/R_S to be as high as practical to minimize the input voltage division. This is a lot to understand at once. Figure 6 shows that the common-collector amplifier works best for (R_S/R_L) ratios less than about 30 when the application is as a small signal input stage with high power gain and for (R_S/R_L) ratios less than about 5 when the application is as a large signal output stage.

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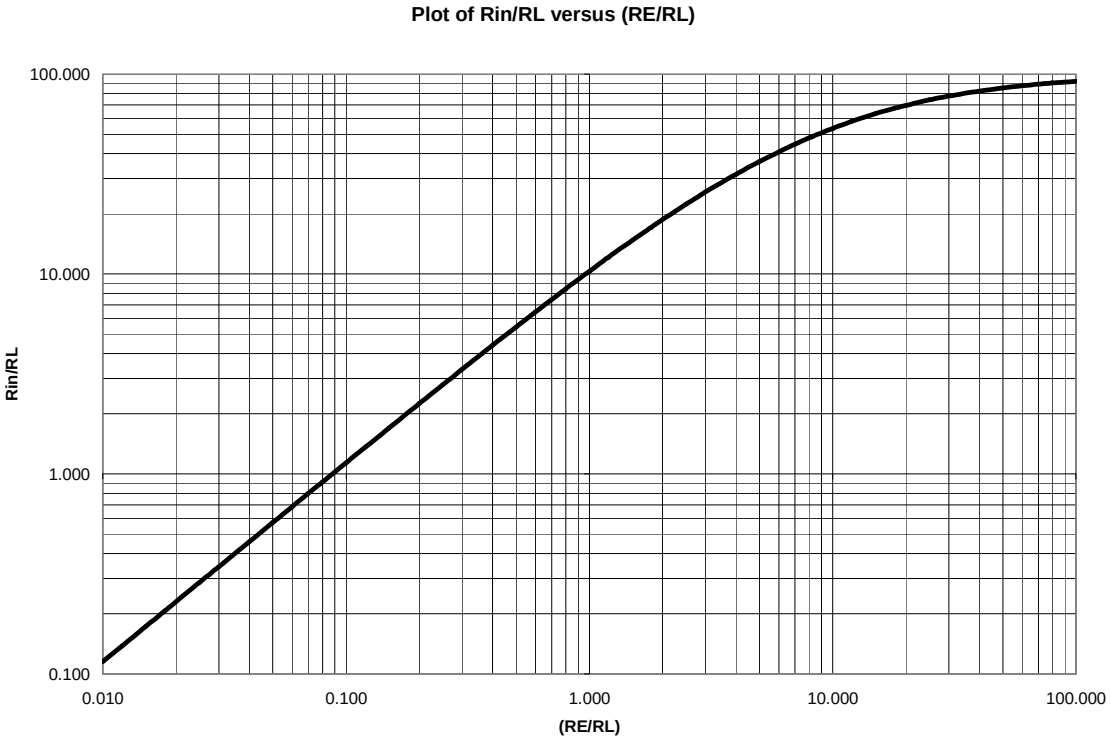

Figure 5: Plot of the typical effect on input resistance that the choice of R_E has

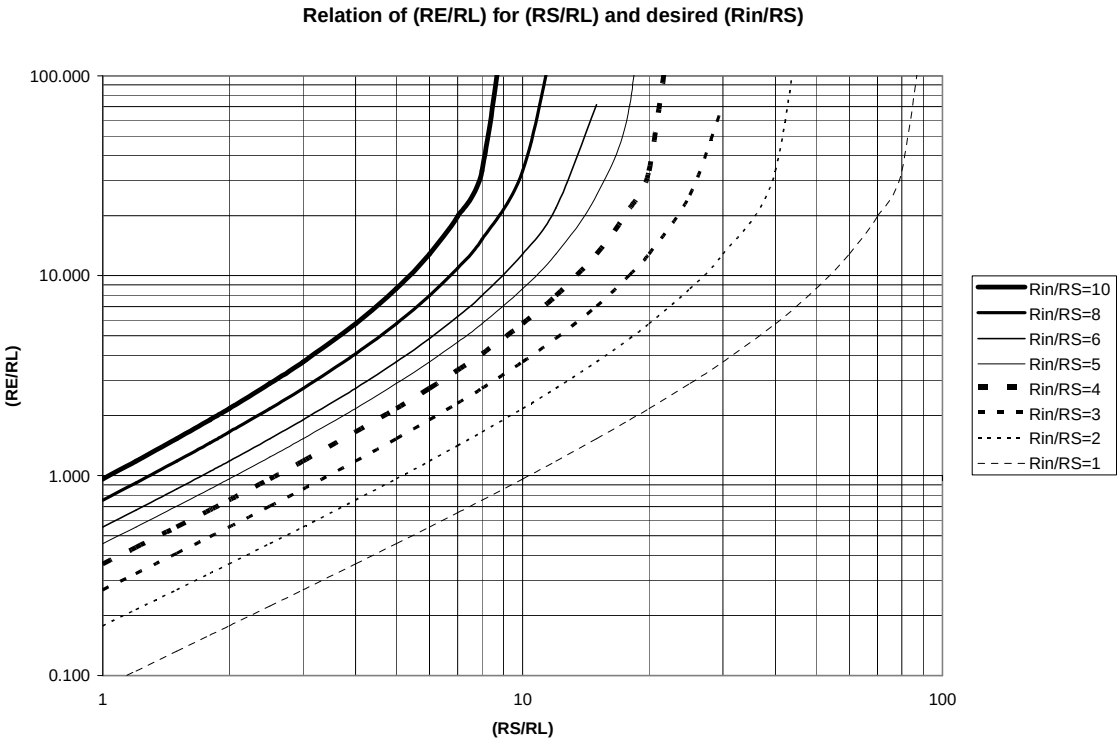

Figure 6: Choosing R_E/R_L for a given R_S/R_L and desired Rin/R_S