Amplifier Frequency Response

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Introduction

All amplifiers have a finite bandwidth. The low cutoff frequency can in some cases extend down to DC and is a parameter under direct control of the designer. The ultimate high frequency limit is determined by the physical characteristics of the components and construction of the circuit. The designer can design to an arbitrary upper cutoff frequency below this limit. The cutoff frequency by definition is the half-power frequency and is the frequency where the power gain is half what it is at a mid-band frequency – i.e. between the lower and upper cutoff frequencies where frequency effects can be ignored.

Amplifiers only need to have sufficient bandwidth to pass the intended or desired signals. Excess bandwidth can be a source of problems as any undesired out-of-band signals are amplified rather than suppressed. As an example, a common myth in audio amplifiers is that bandwidth to hundreds or even thousands of kilohertz is needed for fine audio reproduction. The reality is that it is desirable for an audio amplifier to have a net upper cutoff frequency only slightly higher than the limit of human hearing (about 20 kHz) or the upper cutoff frequency of the speakers – whichever is lower. Individual stages will need a higher frequency response in order for the net to be right as will be seen later. Another myth in audio amplifiers is that the low frequency response should extend down to DC. The reality is that the net low cutoff frequency should only be slightly lower than that of the speakers. Response below what the speakers can reproduce actually causes distortion as the speaker is forced to move beyond its intended limits in a nonlinear way. Well designed audio systems are carefully band-limited for optimum sound quality.

Low Cutoff Frequency

The low cutoff frequency is determined by the size of the coupling capacitors. Direct coupled amplifiers have response down to DC. Each AC coupled stage has an associated series RC time constant with the sum of output resistance of one stage in series with the input resistance of the next stage multiplied by the capacitance of the coupling capacitor. The cutoff frequency is the frequency when the reactance of the capacitance equals the series resistance and at this frequency only half the power is transferred from one stage to the next as compared to the case when the reactance is negligibly small. Figure 1 shows the typical AC coupling circuit.

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$$R = R_o + R_{in}$$
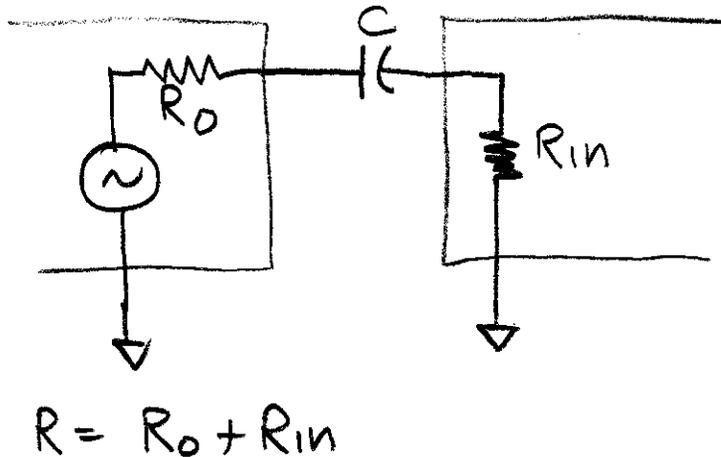
Figure 1: AC coupling, series circuit

The low cutoff frequency is

$$Fcl = 1 / (2 * \pi * Rseries * Cseries) \hspace{3cm} \text{Eq. 1}$$

An amplifier typically has several AC couplings from input to output. The question is how to compute the net low cutoff frequency of a chain of AC coupled stages. Computing the exact cutoff frequency is impractical for hand calculations – the high order math is best done via a computer. For many problems an exact answer is not necessary and a reasonable approximation is fine. A popular approximation is as follows

$$Fcl\_net \sim= sqrt(Fcl1^2 + Fcl2^2 + \ldots Fcln^2) \hspace{2cm} \text{Eq. 2}$$

It should be obvious from Eq. 2 that Fcl_net will always be higher than the highest individual cutoff frequency. Another observation is that the higher cutoff frequencies strongly dominate the result. The accuracy of Eq. 2 is reasonable for most cases and is typically better than twenty percent. The accuracy is worst if most individual cutoff frequencies are nearly the same – the error can be several tens of percent.

The design process is determining the proper size capacitors to use for each coupling in order to achieve the desired net low cutoff frequency. In thinking about how one should distribute the time constants for each coupling the thought should occur to make all time constants the same – thus the low cutoff frequency is identical for all couplings. This concept greatly simplifies what otherwise would be a huge guessing game. From earlier discussion it should be noted that the individual cutoff frequency for each coupling must be lower in order to net a target net low cutoff frequency. The question for the designer is how much lower? Simplistically, one might think that the cutoff frequency should be the target cutoff frequency divided by the number of AC coupling but this turns out to be overkill. Each stage only has to reduce the power transfer by one nth of half. This problem is readily solved via a computer that raises the first order transfer function to the nth power and then solves for the resultant cutoff frequency using numerical methods.

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Since that calculation is always the same a simple table of results can be generated as shown below.

Number of Stages	**Factor of individual cutoff frequency to net cutoff frequency**
1	1.000
2	0.644
3	0.510
4	0.435
5	0.386
6	0.350
7	0.323
8	0.301
9	0.283
10	0.268

Table 1

Table adapted from *Analysis and Design of Integrated Electronic Circuits*, second edition, by Paul M. Chirlian, Harper and Row, 1987, page 589

From Table 1 if we are designing an amplifier that has three AC couplings and we desire a net low cutoff frequency of 100 Hz, then each coupling should have a cutoff frequency of 51 Hz. It is not necessary to hit this exactly and the common tactic is to calculate the require capacitance for each stage and round up to the next standard or convenient capacitor size. This will result in a net cutoff frequency of slightly less than 100 Hz but the interpretation of the design specification should be "not higher than 100 Hz." A little lower cutoff frequency is fine.

AC couplings include stage to stage coupling plus emitter bypass capacitors in common-emitter amplifiers. The resistance for the time constant calculation is that of R_E1 (which might be zero) plus the dynamic emitter resistance, re. The emitter bias resistor, R_E, is also involved but that effect is usually small and is more than compensated by the rounding up to the next larger capacitor size discussed earlier. Figure 2 shows the typical circuit.

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Typically $R_E \gg R_{E1}$

R_{E1} could be 0

$R = r_e + R_{E1}$
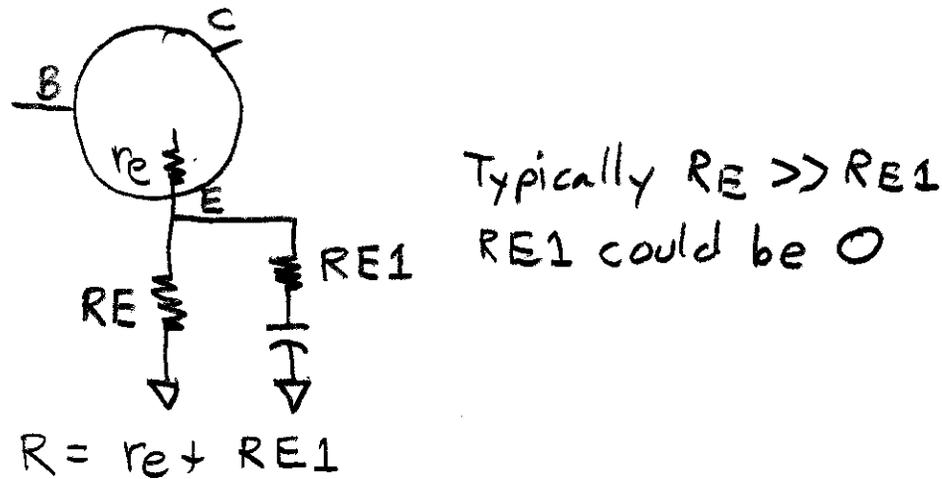
*Figure 2: AC coupling, series circuit in emitter*

It should be noted then that a simple single stage common-emitter amplifier has a total of three AC couplings – the input, the emitter bypass, and the output.

High Cutoff Frequency

The ultimate high cutoff frequency of an amplifier is determined by the physical capacitances associated with every component and of the physical wiring. Transistors have internal capacitances that shunt signal paths thus reducing the gain. The high cutoff frequency is related to a shunt time constant formed by resistances and capacitances associated with a node. We are stuck with the physical capacitances (typically in the single and low double digit picofarrad range) so the primary option for very high frequency response is low value resistances. Another option is much smaller components which in turn have lower capacitances. In some cases, small inductances can built into the circuit to counteract the capacitances. The ultimate in extremely high frequency response is achieved by building the amplifier as a matched transmission line.

Figure 3 shows the typical circuit that becomes significant at high frequencies. Note that Cin could be the sum of several different capacitances. These capacitances are from the physics of the components and construction and are not arbitrary. Only sometimes are these capacitances intentional components

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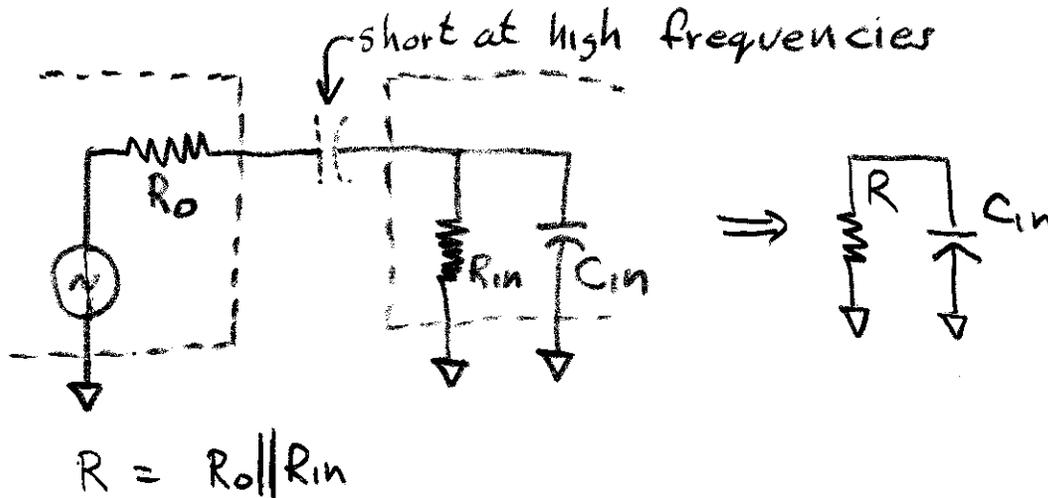
Figure 3: Shunt capacitance at high frequency

The high cutoff frequency of each node of an amplifier is inversely proportional to the net shunt resistance and net shunt capacitance and is given by

Fch = 1 / (2 * π * Rshunt * Cshunt)   Eq. 3

This equation is identical to Equation 1 except that the resistances and capacitances are in shunt rather than in series. A given amplifier will have several high cutoff frequencies. The net high cutoff frequency is a challenge to calculate manually but a popular approximation is

$$Fch\_net \sim= \frac{1}{\sqrt{1/Fcl1^2 + 1/Fcl2^2 + \ldots Fcln^2}}$$ Eq. 4

The Fch_net will always be lower than the lowest individual cutoff frequency. The lower cutoff frequencies will also dominate the result. Like Equation 2, the approximation is generally good to around twenty percent unless most cutoff frequencies are similar – then the accuracy degrades to several tens of percent.

It is often the case that we do not want wide bandwidth in an amplifier and the designer will add capacitance to lower the bandwidth to the desired amount.

The primary discussion here is the internal capacitances of a transistor and how those affect the high frequency response. The transistor internal capacitances are proportional to the physical area of the junctions and inversely proportional to the width of the depletion region, i.e. the classic physics of a capacitor. For a simple transistor model there are only two capacitances we will consider – C_{BC} which is between the base and collector junctions and C_{BE} which is between the base and emitter junction as shown in Figure 4. This means that the capacitance is a function of bias conditions. A forward biased junction has relatively high capacitance (tens to over one hundred picofarrads depending on forward current) because the width of the depletion region is narrow. A

reversed biased junction has relatively low capacitance (typically less than ten picofarrads and even less than one picofarrad in some cases) because the width of the depletion region is wide. These capacitance effects are shown in Figure 5. The fact that junction capacitance is inversely related to reverse voltage is a useful characteristic that is used for electronic tuning of radio frequency networks. For high frequency amplifiers we generally want to operate the transistor with as high a reverse bias on the base-collector junction as practical to minimize that capacitance. This means that V_{CB}min should be greater than 4 volts.
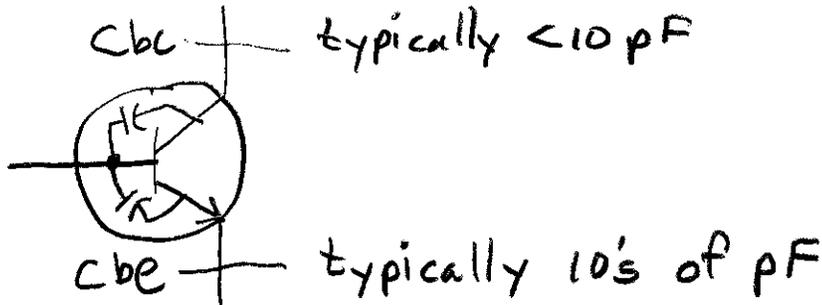

Figure 4: Transistor capacitances
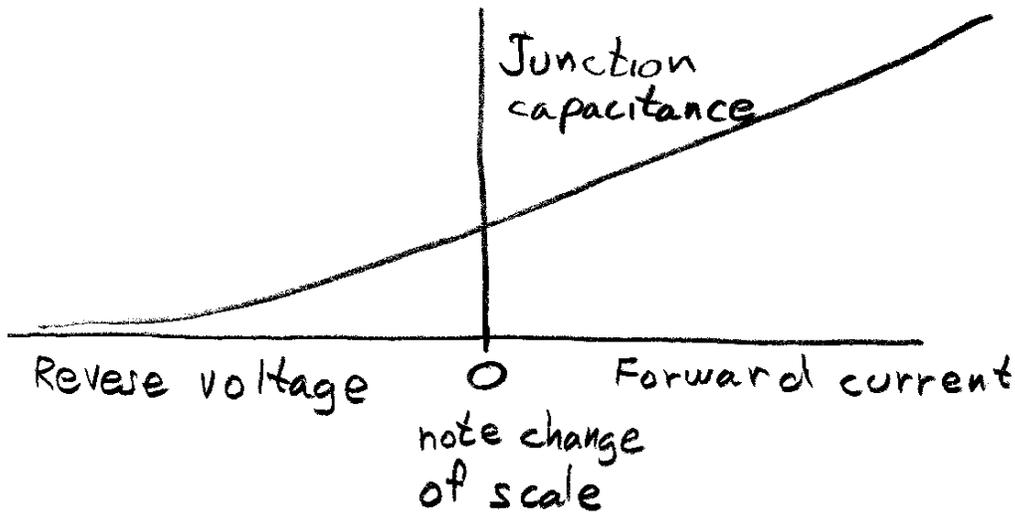
Figure 5: PN junction capacitance curve

The Miller effect

In the early days of vacuum tube amplifiers it was observed that high gain amplifiers built with common-cathode (analogous to common-emitter or common-source) architectures had much lower than expected high frequency response. An engineer whose name was Miller discovered the reason why. The small capacitance that exists

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from the output of the amplifier to the input was magnified by the amplifier gain and appeared as a large shunt capacitance across the input of the amplifier. In those days the capacitance was between the plate and grid which is analogous today to capacitance between the collector and base (i.e. $C_F = C_{BC}$). The Miller effect occurs only in inverting amplifiers – it is the inverting gain that magnifies the feedback capacitance. Note that one side of the capacitor is connected to the input signal and the other side is connected to the larger in magnitude and phase inverted output signal. This causes the reactive current through the capacitor to be ($|Gain| + 1$) higher than what would exist if the feedback capacitance were only across the input – thus the capacitor appears larger by the factor of ($|Gain| + 1$). This causes a significant low frequency pole to exist and limits amplifier bandwidth. Note that the absolute value of gain is used to eliminate sign errors since the actual sign of the gain is minus.


$$C_{in} = (|A| + 1) C_F$$

$$i_{in}(s) \frac{V_{in}(s)}{\frac{1}{C_F s}} - \frac{(-A V_{in}(s))}{\frac{1}{C_F s}} = V_{in}(s) (|A| + 1) C_F$$
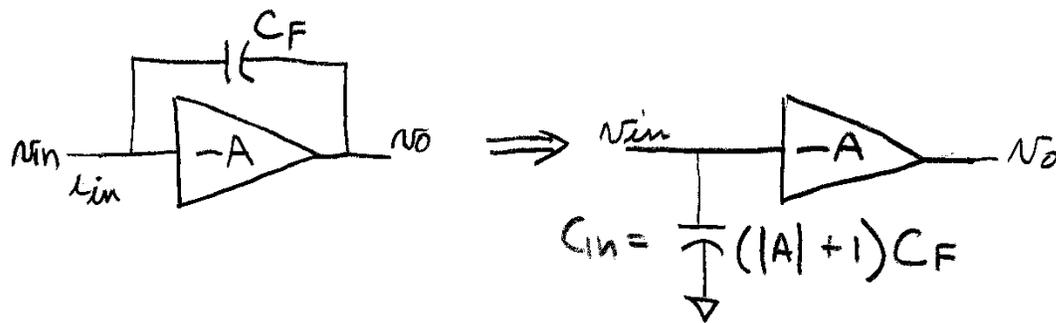
$$Z_{in}(s) = \frac{V_{in}(s)}{i_{in}(s)} = \frac{1}{(|A| + 1) C_F s} \qquad C_{in} = (|A| + 1) C_F$$
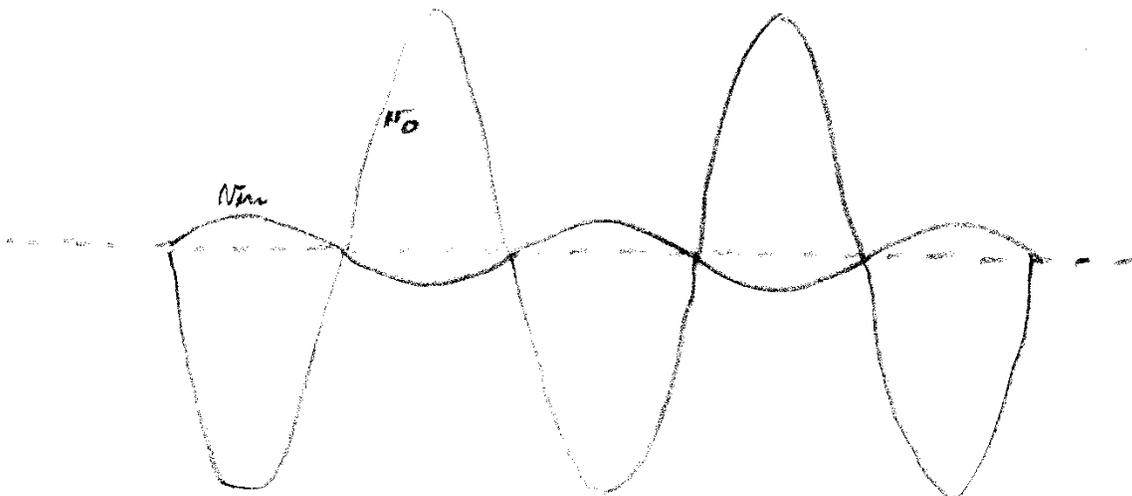
Figure 6: Miller effect

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An example problem

The transistor circuit in Figure 7 will be analyzed for low and high cutoff frequencies. Note that this is the circuit you will build and measure in Lab 6. The summary results from bias analysis and AC analysis are shown. We use the results from AC analysis to do frequency response analysis. Note that a significant value for C_{BC} has been inserted to arbitrarily lower the high frequency bandwidth.
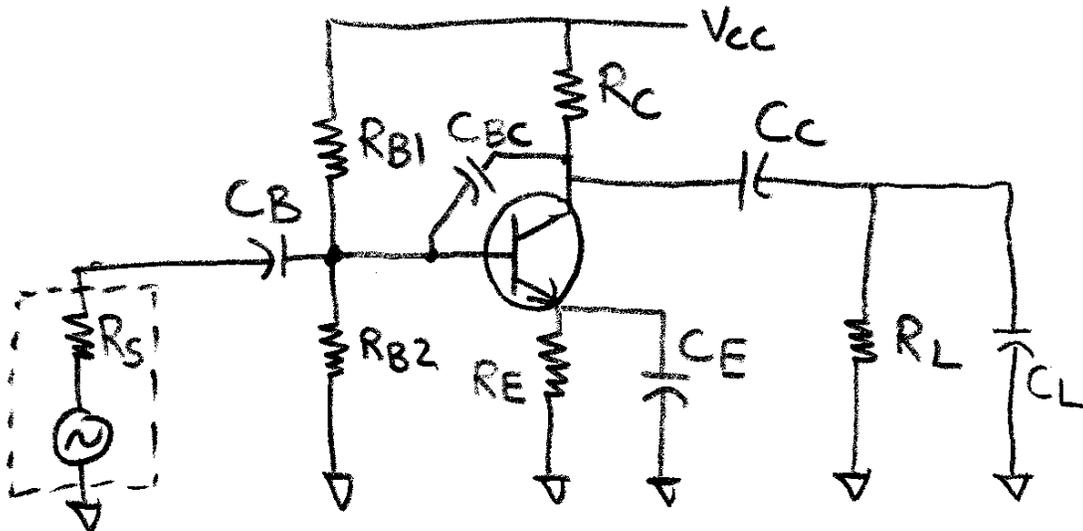

Figure 7: Example circuit

$V_{CC} = 12V$, $R_S = 1K$, $R_B1 = 150K$, $R_B2 = 22K$, $R_E = 1.5K$, $R_C = 10K$, $R_L = 10K$,
$C_B = 1$ uF, $C_E = 100$ uF, $C_C = 0.1$ uF, $C_{BC} = 22$ pF, $C_L = 470$ pF,
Not shown are: $C_{BE} = 25$ pF (assumed internal to transistor), Cin_stray = 25 pF, and Co stray = 20 pF – these are assumed wiring capacitances.

Summary bias and AC analysis using B = 150 and $V_{BE} = 0.65$
$V_{BB} = 1.53$ V
$R_B = 19.2$ K
$I_E = 544$ uA
$I_C = 540$ uA
$V_C = 6.6$ V
$r_e = 48$ ohms
rbt = 7.3K
$R_{in} = 5.25$ K
$R_o = 10K$
Av = -208
Avl = -104

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Low Frequency Analysis

Fcl1 = 1 / (6.28 * (1K + 5.25K) * 1 uF) = <u>25.5 Hz</u>

ret = 48 + 19.2K||1K/151 = 54.1

RE || ret = 1500|54.1 = 52.2

Fcl2 = 1 / (6.28 * (52.2 + 0) * 100 uF) = <u>30.5 Hz</u> (note: RE1 = 0)

Fcl3 = 1/(6.28 * (10K + 10K) * 0.1 uF) = <u>79.6 Hz</u>

Fcl_net ~= sqrt(25.5^2 + 30.5^2 + 79.6^2) = **88.9 Hz**

High Frequency Analysis

Cmiller = 22 pF * (104 + 1) = 2.31 nF   (note that we use Avl and C_{BC})

Cin_total = 2.31nF + 25 pF + 25 pF = 2.36nF (note how Cmiller dominates)

Rin_shunt = 1K || 5.25K = 840 ohms

Fch1 = 1 / (6.28 * 840 * 2.36 nF) = <u>80.37 kHz</u>

Cout_shunt = 20 pF + 470 pF = 490 pF

Ro_shunt = 10K || 10 K = 5K

Fch2 = 1 / (6.28 * 5K * 490 pF) = <u>67.7 kHz</u>

Fch_net ~= 1 / (sqrt(1/80.37 kHz^2 + 1/67.7 kHz^2) = **51.8 kHz**