JFET AC Design

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Introduction

The process of performing AC amplifier design using the JFET transistor involves

1. Determining the appropriate type (CS, CD, CG) of amplifier to use
2. Choosing certain resistor values based on the load resistance
3. Determining appropriate bias conditions for the type of amplifier being designed
4. Performing DC bias design to achieve those conditions
5. Calculating the necessary value of R_{S1} to achieve a specific gain. (Common-source only)
6. Determining the value of AC coupling capacitors to achieve a specified low frequency response

Step 6 will not be discussed here as the details will be in another note. This paper is concerned with determining resistor values only.

It is possible that a desired gain may not be achievable. This will not be known until some calculation produces a negative resistor value.

Each type of amplifier will have different issues to consider.

The choice of amplifier type

The three different types of amplifiers; common-source, common-gate, and common-drain have very different characteristics. For any given amplifier requirement, one of these types will be the best choice although a different type may also perform well. In general, the best amplifier to use is the one whose input resistance is comparable to the source resistance and whose output resistance is comparable to the load resistance. It is usually not possible to satisfy both input and output resistance characteristics simultaneously. Sometimes it is necessary to perform the design for two of the three possible types to see which one ends up providing the best overall characteristics. Here are some rough guidelines when the goal is to achieve high power gain.

Source resistance / load resistance	**Good choices to consider**
greater than 1	Common-source or Common-drain
0.1 to 1	Common-source
less than 0.1	Common-gate

It can be shown that the common-source amplifier is capable of achieving the highest possible power gain if it is a good choice for the given source/load resistance. Even when

it is the best choice, the common-gate is not capable of the power gain of a common-source amplifier. Although when the common-gate amplifier is the best choice, the power gain achieved is higher than if a common-source amplifier were used. The common-drain amplifier is also capable of very high power gain because of large ratio of input to output impedance possible. Overall, the common-source amplifier is the most flexible in terms of input and output resistance while also achieving reasonable power gain. The common-gate amplifier is generally only useful when the source resistance is much smaller than the load resistance. This is often the case in high frequency circuits. The common-drain amplifier is used when it is desirable to have low output impedance.

Stability of design issues

Stability as used here refers to the desirable characteristic that bias voltages and currents are little affected by changes in temperature or variations in I_{DSS} or V_P from transistor to transistor. Stability and power gain can be in opposition to each other thus requiring compromise or engineering judgment to resolve.

Determining the JFET parameters to use for design

Design can not be completed without knowing I_{DSS} and V_P. The JFET must be selected based on a suitable value of I_{DSS} for the given load resistance. There is then little if any choice on V_P. The value that comes with a particular choice for I_{DSS} must be used. The spread of I_{DSS} and V_P is very wide for a given type of JFET. The design is best done using the minimum value for I_{DSS}. The design should be checked at the maximum values to confirm acceptable operation.

Common-source design

The first step in the design process is to choose an R_D based on the load resistance. Values that work well are generally in the range: $R_L/2 <= R_D <= 2 * R_L$.

The second step is to determine a suitable value for V_{DQ}. A middle value to use is $(V_{GG} + V_{DD}) / 2$ although higher or lower values can be used for specific reasons. There is no optimum value for all situations. Lower values (but not too low) for V_{DQ} require higher drain currents and thus achieve higher voltage and power gain.

The third step is to calculate the drain current based on the first two steps:
$I_{DQ} = (V_{DD} - V_{DQ}) / R_D$.

The fourth step is to choose a JFET with an appropriate minimum I_{DSS} for the drain current computed in step three. The minimum I_{DSS} should generally be roughly twice I_{DQ}. Unless the desired signal amplitudes are very small, the JFET should not be biased at I_{DSS}

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because voltage excursions that increase drain current begin to forward bias the gate-channel junction. Thus, I_{DQ} is generally chosen to be less than I_{DSS}max such that the maximum positive excursion does not cause I_D to exceed I_{DSS}max. There is no optimum value for all situations. The designer must choose an appropriate value.

The fifth step is then to complete the bias design. This means computing R_S and selecting a standard resistor value.

The sixth step is to choose R_G. A popular value is 1,000,000 Ohms but any reasonable value may be used.

The seventh step is to determine the value of R_{S1} if the gain is to be a specific value instead of the maximum possible (i.e. $R_{S1} = 0$), then R_{S1} can be calculated as follows using the magnitude (dropping the minus sign) of the desired gain. This method ignores any input voltage division as it is assumed that that value is very near unity.

Note that the equation for voltage gain can be written as:

$|\text{gain}| = \text{numerator} / (1/g_m + R_S')$

where:
|gain| is the magnitude of the gain

numerator is either R_D if the gain is the unloaded stage gain or $R_D||R_L$ if the gain is the loaded stage gain.

R_S' is $R_S||R_{S1}$

Rearranging the equation we have:

$R_S' = (\text{numerator} / |\text{gain}|) - 1/g_m$

Then, $R_{S1} = R_S * R_S' / (R_S - R_S')$

The design is now complete.

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Common-gate design

The design of common-gate amplifiers is very similar to the design of common source amplifiers. Steps one through five are identical. In step six, since R_G is not in parallel with the signal input, it can be chosen arbitrarily small. In step seven, R_{S1} could be added for the purpose of raising the input impedance of the amplifier although at the expense of reduced voltage gain. This is so rarely done that the computations will not be discussed here.

Common-drain design

The designer does not have control over the gain of a common-drain design. The gain will always be less than one. Typical gains vary from about 0.99 down to 0.3 or below. The power gain can be very large because the input impedance can be in the millions of Ohms while the output impedance is generally in the hundreds of Ohms.

The first step is to choose a JFET with a maximum I_{DSS} appropriate for the desired output amplitude across the load resistance. One problem with using a resistor (R_S) for biasing the JFET to a desired operating current is that R_S is in parallel with the load resistance and this resistance value might be small (if V_{GG} is zero) compared to the load thus causing an unwanted voltage division. One common way around this problem is to replace R_S with a current sink of the desired operating current. Then, the effective resistance value is very large and no unnecessary voltage division occurs.

An alternative to the current sink is to choose R_S between about half and twice the load resistance. Then compute the required V_{GG} to bias the JFET to the desired operating current. V_{GG} will now be derived from a voltage divider between V_{DD} and ground. The sequence of steps is as follows. First, choose R_S based on the load resistance. Second, choose an appropriate I_{DQ} for the desired signal amplitudes. Third, calculate $V_S = I_{DQ} * R_S$. Fourth, calculate V_{GS} required for the desired I_{DQ}. Fifth, calculate $V_{GG} = V_S + V_{GS}$. Sixth, determine the appropriate voltage divider from V_{DD} to produce V_{GG}.