**JFET Bias Analysis**

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**Introduction**

The purpose of bias analysis is to determine the drain current of the JFET. Once the drain current is known then all other bias voltages can be calculated. The general circuit is shown in Figure 1. In many cases, the actual circuit will have only a single voltage source. Circuits can vary a bit so the first step is to transform whatever circuit is being analyzed into the form of Figure 1.

![Figure 1: General JFET circuit for bias analysis](image)

**Development of the procedure**

The basic equations written by inspection of Figure 1 are:

- \( V_G = V_{GG} \) since we take \( I_G \) to be 0 \[ Eq. 1 \]
- \( V_S = V_{SS} + I_D \cdot R_S \) \[ Eq. 2 \]
- \( V_D = V_{DD} - I_D \cdot R_D \) \[ Eq. 3 \]
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The drain current and the gate-source voltage are interrelated. If we know one then the other is easily calculated. The problem is that in Equations 1, 2, and 3 we know neither. The usual approach in solving this type of problem is to develop two different equations that represent the same variable related to the one we want to solve for. The equations are then set equal to each other which eliminates the related variable leaving just the desired variable in a single equation that we can solve. To determine \( I_D \), we will substitute basic JFET terminal relationships into Equations 1, 2, and 3.

\[
V_{GS} = V_G - V_S = V_{GG} - (V_{SS} + I_D \times R_S)
\]

Eq. 4

Substituting a basic JFET relationship for \( V_{GS} \) gives

\[
V_{GS} = V_P \times [1 - \sqrt{I_D/I_{DSS}}] = V_{GG} - V_{SS} - I_D \times R_S
\]

Eq. 5

It is now possible to solve Equation 5 for \( I_D \)

\[
V_P \times \sqrt{I_D/I_{DSS}} = V_{GG} - V_{SS} - V_P - I_D \times R_S
\]

Eq. 6

\[
V_P^2 \times I_D/I_{DSS} = (V_{GG} - V_{SS} - V_P - I_D \times R_S)^2
\]

Eq. 7

It is obvious that expanding Equation 7 will be quite messy. Before proceeding it is useful to realize that the constant terms can be combined into simple constants.

Let \( V_K = V_{GG} - V_{SS} - V_P \)

Eq. 8

Let \( V_R = V_P^2/I_{DSS} \) which has units of voltage * resistance

Eq. 9

Now Equation 7 can be written more simply as

\[
V_R \times I_D = (V_K - I_D \times R_S)^2
\]

Eq. 10

Expanding Equation 10 produces the quadratic equation:

\[
R_S^2 \times I_D^2 - (2 \times V_K \times R_S + V_R) \times I_D + V_K^2 = 0
\]

Eq. 11

Solving the quadratic equation for \( I_D \) gives:

\[
I_D = \frac{-2 \times V_K \times R_S + V_R \pm \sqrt{[(2 \times V_K \times R_S + V_R)^2 - 4 \times R_S^2 \times V_K^2]}}{2 \times R_S^2}
\]

Eq 12

Equation 12 looks messy but there are some simplifications that can be done. Of the two possible solutions to Equation 12, only the negative root produces a valid \( I_D \). Also, with the squaring and square root, some sign information is lost. We will have to adjust the sign of the result to agree with reality. Factoring out a common term produces:
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\[
I_D = \frac{(V_R)}{(2 * R_S^2)} \times \frac{[2 * V_K * R_S]}{[\sqrt{(4 * V_K * R_S + 1)}]}
\]

Eq. 13

Equation 13 can be simplified further by making the following substitution:

\[
X = \frac{|2 * V_K * R_S|}{V_R}
\]

Eq. 14

The purpose of the absolute value signs is to make the calculation independent of whether an n-channel JFET or a p-channel JFET is being used as discussed below. Note that the numerator has units of voltage * resistance and that the denominator term has units of voltage * resistance as discussed earlier. Thus, Equation 14 has no dimension.

Substituting Equation 14 into Equation 13 gives:

\[
I_D = \frac{(V_R)}{(2 * R_S^2)} \times \left[ X + 1 - \sqrt{2 * X + 1} \right]
\]

Eq. 15

Equation 15 is the solution we have been seeking but there are some sign issues that must be dealt with. Note that \(V_R\) will be positive for n-channel JFETS and negative for p-channel JFETS. The constant, \(X\), must be a positive number regardless of whether the JFET is N-channel or P-channel so we will use the absolute value of \(X\). Now, looking at the expression inside the \([\]\) of Equation 15, it is obvious that that expression will always produce a positive result. Thus, for n-channel JFETs, \(I_D\) will be positive as it should and for p-channel JFETs, \(I_D\) will be negative as it should.

If \(R_S\) is 0 then Equation 15 will give the correct answer if a very small (say 0.01 Ohm) resistance is substituted for \(R_S\). Or, in the special case when \(R_S\) is 0, one of the fundamental relations for the JFET can be used instead since the complexity of dealing with \(R_S\) is gone.

\[
I_D = I_{DSS} \times [1 - (V_{GS}/V_P)]^2 \quad \text{if } R_S = 0
\]

Eq. 16
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The sequence of steps to calculate the bias conditions is as follows:

1. Transform the actual circuit into the general form of Figure 1. The result of this is to establish: $V_{DD}$, $V_{SS}$, $V_{GG}$, $R_D$, $R_S$, and $R_G$.
2. Determine the $I_{DSS}$ and $V_P$ that will be used in the analysis. The analysis might be repeated for different values over the spread for a given JFET.
3. Use Equation 8 to calculate $V_K$ if $R_S$ is not zero
4. Use Equation 9 to calculate $V_R$ if $R_S$ is not zero
5. Use Equation 14 to calculate $X$ if $R_S$ is not zero
6. Use Equation 15 to calculate $I_D$ if $R_S$ is not zero
7. Or, use Equation 16 to calculate $I_D$ if $R_S$ is zero
8. Use Equation 1 to calculate $V_G$
9. Use Equation 2 to calculate $V_S$
10. Use Equation 3 to calculate $V_D$

The analysis is now complete but we must check to make sure that the JFET is operating in the active region. Otherwise, the JFET is not working per our model and our bias calculations are wrong.

The JFET is in the active region if

1. $(V_D - V_S) > (V_G - V_S - V_P)$
   which reduces to $V_D > (V_G - V_P)$ noting that $V_P$ is negative for n-channel

   and

2. $0 < [(V_G - V_S) / V_P] < 1$  
   $V_{GS}$ must have the same sign as $V_P$

As a reality check,

3. $0 < I_D/I_{DSS} < 1$  
   $I_D$ must have the same sign as $I_{DSS}$

A very common error is to use the wrong signs for $I_{DSS}$ and $V_P$. The correct signs are as follows:

<table>
<thead>
<tr>
<th>JFET type</th>
<th>$I_{DSS}$</th>
<th>$V_P$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-channel</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>P-channel</td>
<td>-</td>
<td>+</td>
</tr>
</tbody>
</table>

Figure 2 illustrates some common JFET circuits and the necessary transformations to be of the form in Figure 1.
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Figure 2: Common JFET circuits