JFET Bias Design

by Kenneth A. Kuhn
Nov. 5, 2008, rev. July 28, 2009

Introduction

These notes provide the basic information to design JFET amplifiers that will operate over the wide range of parameters for a particular JFET part number.

Bias Design

The goal of bias design is to obtain a desired drain quiescent current, I_{DQ}. Ideally, this current does not vary too much with the wide spread in device parameters, I_{DSS} and V_P. In the data sheet the minimum and maximum values for I_{DSS} are given and often are spread over a range of between about four and ten to one. The minimum and maximum values for V_P are also provided and those typically vary over a range of between about three and seven to one. There is a fairly strong correlation between the minimum I_{DSS} and the minimum V_P. Also, there is a fairly strong correlation between the maximum I_{DSS} and the maximum V_P. This fact helps a lot and will be used in the design process. These values will be referred to as: I_{DSS}min, $V_P$min, I_{DSS}max, $V_P$max. Note that the magnitudes establish the minimums and maximums as sign information is not meaningful for this.

There are two circuit methods to accomplish the desired bias. The first method as shown in Figure 1 (left) is to connect the source lead to ground and apply a gate bias voltage from V_{GG} through a series resistor, R_G. Although very simple, this method is very sensitive to the spread in device parameters. The second method as shown in Figure 1 (right) is to place a resistor, R_S, in series with the source terminal and connected to a supply, V_{SS}. The gate bias voltage is applied from V_{GG} through a series resistor, R_G. This method has much more flexibility and can minimize the sensitivity to the spread of device parameters. There are two options. One is to set V_{GG} to a particular voltage and calculate the required value for R_S. The second method is to set R_S to a particular resistance and calculate the required value for V_{GG}. The method to use depends on what is more convenient.

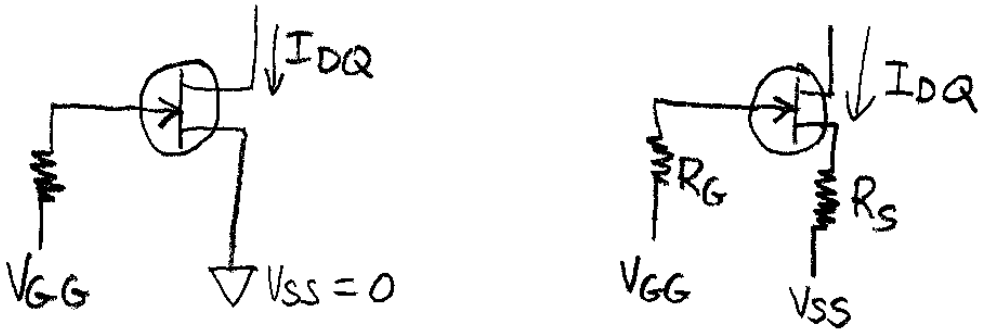

Figure 1: JFET Bias Circuits

JFET Bias Design

We must always base the design on the minimum (magnitude) values for I_{DSS} and V_P. However, the circuit must operate satisfactorily at the maximum values for I_{DSS} and V_P. We do not have much control over this second aspect. Our procedure is to design for the minimums and then verify performance at the maximums. If the circuit does not work properly at the maximums then we revise our design and try again. Design is often an iterative process and JFET bias design is more challenging because of the wide spread in parameters.

Case 1: RS = 0

For any case, the required value of V_{GS} to achieve the chosen I_{DQ} is calculated as

$V_{GS} = V_P\text{min}*(1 - \text{sqrt}(I_{DQ} / I_{DSS}\text{min})$ Eq. 1

where I_{DQ} is less than or equal to I_{DSS}min.

For the first case, V_{GG} is simply equal to V_{GS} since the source terminal is at zero potential. When the design is checked using the maximum parameter values the drain current will typically be much higher and may cause the value of the drain voltage, V_D to be too low ($V_{DD} - I_{DSS}\text{max} * R_D$) for the circuit to work if there is any resistance in the drain circuit. The second case circuit can be designed to significantly reduce the variation in I_{DQ} with parameter variation.

Case 2A: Calculating the required V_{GG} for a given value of R_S

We first calculate the required value of V_{GS} using Equation 1 for a selected value for R_S. Then we note that the voltage, V_S, at the source terminal is:

$V_S = V_{SS} + I_{DQ} * R_S$ Eq. 2

The voltage at the gate terminal, V_G, then must be $V_S + V_{GS}$. Thus,

$V_{GG} = V_S + V_{GS}$ Eq. 3

Substituting Equation 2 gives

$V_{GG} = V_{SS} + I_{DQ} * R_S + V_{GS}$ Eq. 4

Keep in mind that V_{GS} is a negative value for n-channel JFETS.

Case 2B: Calculating the required R_S for a given value of V_{GG}

The calculation of the required value of R_S for a selected value for V_{GG} is obtained by substituting Equation 3 into Equation 2 as follows.

$V_{GG} - V_{GS} = V_{SS} + I_{DQ} * R_S$ Eq. 5

Solving for R_S gives.

$R_S = (V_{GG} - V_{GS} - V_{SS}) / I_{DQ}$ Eq. 6

Remember that V_{GS} is a negative value for n-channel JFETs – this is easy to forget. It is not uncommon that V_{GG} and V_{SS} are zero in many circuits. Equation 6 gives the required value of R_S in what is known as the self-bias circuit. The self-bias circuit is popular for its simplicity but is very sensitive to the spread of the JFET parameters. The least sensitive result is obtained when the difference between V_{GG} and V_{SS} can be maximized thus making R_S large (ideally, R_S is a current sink).

Choosing I_{DQ}

If the signal amplitude is in the millivolt level or below then the quiescent drain current is often chosen to be close to I_{DSS}min for the purpose of maximizing the amplifier gain. If the signal level is relatively large then the quiescent drain current is typically chosen to be around three fourths, give or take, of I_{DSS}min to allow for signal swing either side of the bias level. A more detailed discussion is in the note, *Distortion in JFET Amplifiers*.

Some example designs

A particular JFET has I_{DSS}min = 2 mA, I_{DSS}max = 20 mA, $V_P$min = -2 Volts, and $V_P$max = -6 Volts. The power supplies for the common source circuit are V_{DD} = 10 Volts and V_{SS} = -10 Volts. Design the amplifier for a quiescent drain current of 1.5 mA using the methods for case 2 using Figure 1 (right). For V_{GG} chosen to be 0.0 Volts, the required V_{GS} using the minimum parameters is -0.268 Volts. The calculated value of R_S is 6845 ohms which is rounded to the standard value of 6800 ohms. The variation in drain current is from 1.51 to 2.07 mA over the spread of JFET parameters. The g_m varies from 0.00174 to 0.00214 S.

For an alternate design choosing R_S to be 7500 ohms the calculated value of V_{GG} is 0.98 volts. The variation in drain current is from 1.5 to 2.5 mA over the spread of JFET parameters. The g_m varies from 0.00173 to 0.00212 S.

For reference, the design is repeated for the simplistic case 1 and V_{GG} is -0.268 volts. The variation in drain current is from 1.5 to 10.7 mA – a huge spread. The g_m varies from 0.00173 to 0.0049 S – also a huge spread.

The design done for the self-bias case where $V_{GG} = V_{SS} = 0$ results in an R_S of 180 ohms. The variation in drain current is from 1.5 to 10 mA over the spread of JFET parameters. The g_m varies from 0.00173 to 0.0047 S. Although convenient, it is clear from these examples that the self-bias case is very sensitive to device parameters.

JFET Bias Design

Common-source specifics

The value of the drain resistance must not be too large or the drain voltage may become too small for JFET stage to work with devices that have high I_{DSS} and V_P. Remember that V_D must be greater than $V_G - V_P$ for the JFET to be in current saturation. The maximum resistance for small signal amplifiers is

$$R_D max = (V_{DD} - V_G + V_P max) / I_D max \qquad \text{Eq. 7}$$

where $I_D max$ is calculated from the circuit design using $V_P max$ and $I_{DSS} max$. If larger signals are involved then $R_D max$ must be reduced so that the negative maximum signal peak does not go below the minimum value for V_D.

Common-drain specifics

For common-drain amplifiers it is desirable to make R_S as large as possible consistent with the JFET remaining in the proper region of operation for the largest signals. This means that V_{GG} will be chosen as high as possible. The highest voltage that can be used is given by the following equation.

$$V_{GG} max = V_{DD} - |V_P| - peak\_maximum\_signal \qquad \text{Eq. 8}$$

R_S is then calculated as usual from this V_{GG}.

Choosing a particular JFET

JFETS are available with IDSS ranging from less than one milliampere up to around one hundred milliamperes. It is hard to provide a concise rule because there are so many varied applications but in general the JFET with the lowest maximum IDSS that can perform the intended job is selected although this is not a strong driver. However, the selection from the manufacturers is very coarse. Since it is hard to know in advance what is the best it is normal to do a design for several different JFETS and examine the resulting issues and then select the best. As has been previously stated, design is often an iterative process.