JFET Homework

Nov. 4, 2007, rev. Nov. 12, 2015

These homework problems provide practice with analysis and design involving the most common type of JFET circuits. There is one problem for each type of circuit. Answers are provided on the last page so the student can verify understanding. Note that some thought in addition to equations is required to solve some problems. All problems are based on a 2N3819 n-channel JFET. This is a very similar part (except for different pin outs you probably could not tell them apart) to the MPF102 used in lab. Summary specifications are below. One way to know for sure that what you are doing with these problems is right is to build some sample circuits in lab. Nothing beats hands-on experience.

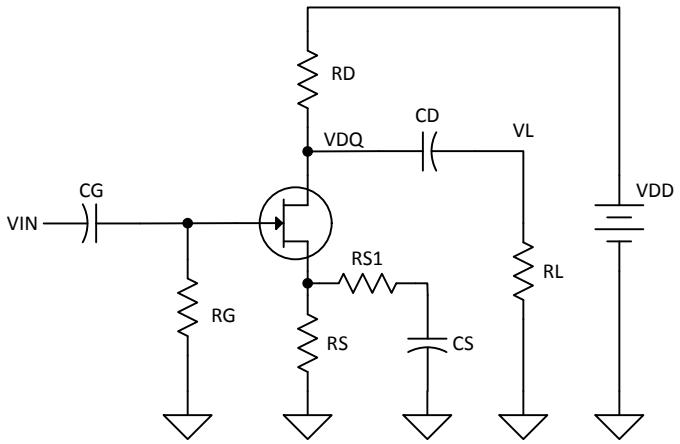
Summary 2N3819 Specifications

	Min	Typ.	Max	Unit
$\mathbf{I_{DSS}}$	2	10	20	mA
$\mathbf{V_P}$	-0.9	-3	-8	Volts

Notes:
Av = unloaded voltage gain.
Avl = loaded voltage gain.
Assume voltage divider for V_{GG} has negligibly small resistance compared to R_G.
Use standard resistor values.

Analysis problems

1. Analyze the following circuit for operation at the low, typical, and high values of the JFET specifications. Determine I_D, V_{GS}, V_D, V_G, V_S, g_m, Av, Avl, and power gain in dB.



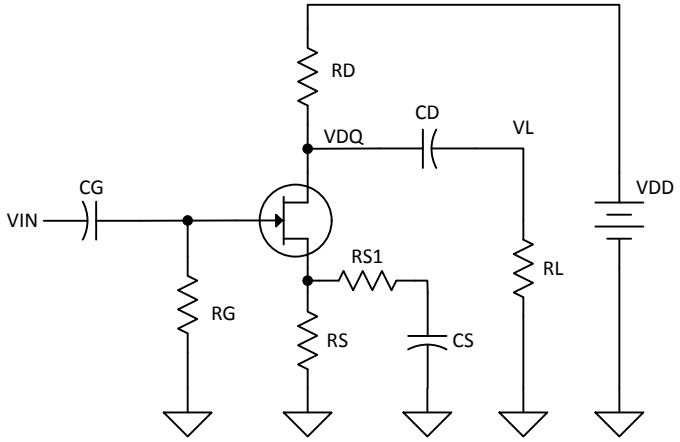
V_{DD} = 20 volts, R_D = 680, R_L = 470, R_G = 1M, R_S = 100, R_{S1} =22

JFET Homework

Answers for Min, Typ, and Max

ID	VGS	VD	VG	VS	gm	Av	Avl	Pg (dB)
0.00142	-0.142	19.04	0.00	0.14	0.00374	-2.385	-0.975	33.056
0.00626	-0.626	15.74	0.00	0.63	0.00528	-3.276	-1.339	35.813
0.01373	-1.373	10.67	0.00	1.37	0.00414	-2.621	-1.071	33.876

2. Analyze the following circuit for operation at the low, typical, and high values of the JFET specifications. Determine I_D, V_{GS}, V_D, V_G, V_S, g_m, Av, Avl, and power gain in dB. This is a different way of implementing problem 1. Note how the characteristics are more stable with device variation than in the first problem.



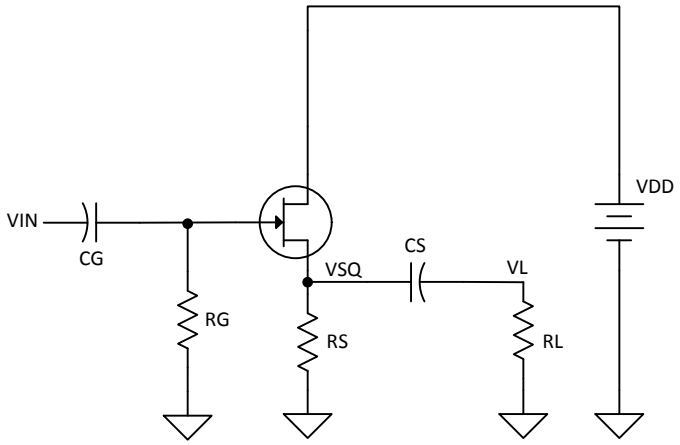
V_{DD} = 20 volts, R_D = 680, R_L = 470, R_G = 1M, R_S = 1.8 K, R_{S1} = 22
R_A = 75 K, R_B = 10 K.

Answers for Min, Typ, and Max

ID	VGS	VD	VG	VS	gm	Av	Avl	Pg (dB)
0.00139	-0.150	19.05	2.35	2.50	0.00371	-2.332	-0.953	32.862
0.00219	-1.595	18.51	2.35	3.95	0.00312	-1.988	-0.813	31.476
0.00381	-4.508	17.41	2.35	6.86	0.00218	-1.417	-0.579	28.535

JFET Homework

3. Analyze the following circuit for operation at the low, typical, and high values of the JFET specifications. Determine I_D, V_{GS}, V_D, V_G, V_S, g_m, Av, Avl, and power gain in dB. See problem 5 for an improved version of this circuit.

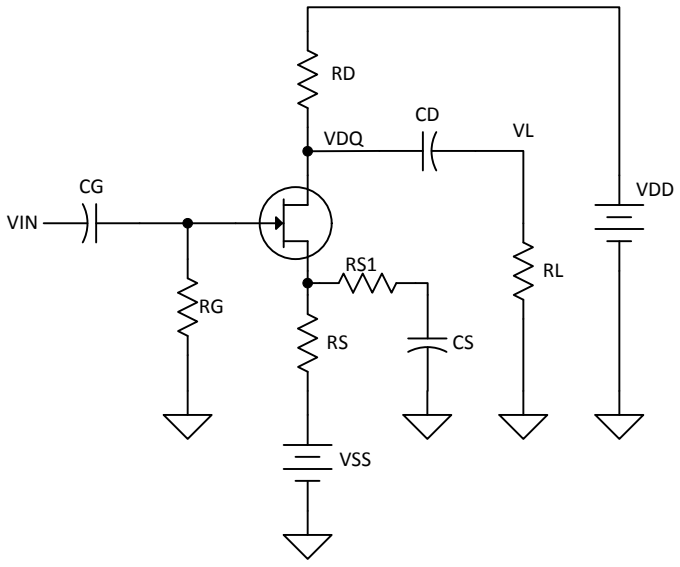


V_{DD} = 20V, R_S = 100 Ohms, R_L = 470 Ohms, R_G = 1 M.

Answers for Min, Typ, and Max

ID	VGS	VD	VG	VS	gm	Av	Avl	Pg (dB)
0.00142	-0.142	20.00	0.00	0.14	0.00374	0.272	0.236	20.733
0.00626	-0.626	20.00	0.00	0.63	0.00528	0.345	0.303	22.911
0.01373	-1.373	20.00	0.00	1.37	0.00414	0.293	0.255	21.396

4. Analyze the following circuit for operation at the low, typical, and high values of the JFET specifications. Determine I_D, V_{GS}, V_D, V_G, V_S, g_m, Av, Avl, and power gain in dB. Observe that this is similar to problem 2 except that the circuit is even more stable because of the larger voltage drop across R_S – i.e. more like a constant current.



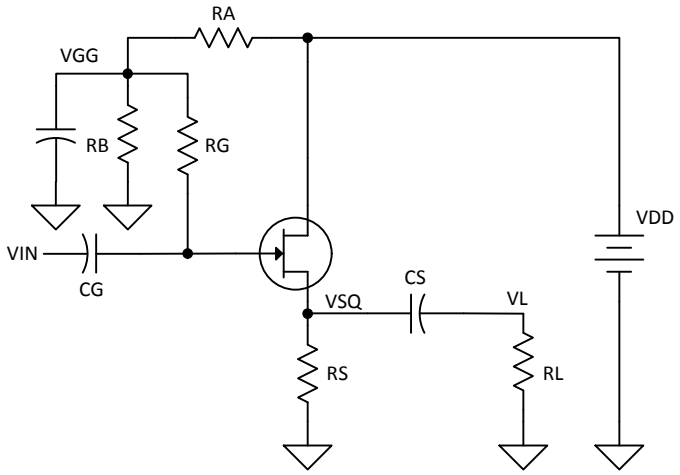
JFET Homework

V_{DD} = 20V, V_{SS}=-2.5 V, R_S = 1.8 K, R_D=680 Ohms, R_L = 470 Ohms, R_G = 1 M, R_{S1} = 22 Ohms.

Answers for Min, Typ, and Max

ID	VGS	VD	VG	VS	gm	Av	Avl	Pg (dB)
0.00146	-0.131	19.01	0.00	0.13	0.00380	-2.386	-0.975	33.062
0.00226	-1.573	18.46	0.00	1.57	0.00317	-2.017	-0.824	31.603
0.00388	-4.478	17.36	0.00	4.48	0.00220	-1.429	-0.584	28.605

5. Analyze the following circuit for operation at the low, typical, and high values of the JFET specifications. Determine I_D, V_{GS}, V_D, V_G, V_S, g_m, Av, Avl, and power gain in dB. Observe that this circuit is more stable and works better than in problem 3



V_{DD} = 20V, R_S = 2.4 K, R_L = 470 Ohms, R_G = 1 M, R_A = 51 K, R_B = 10 K.
Answers for Min, Typ, and Max

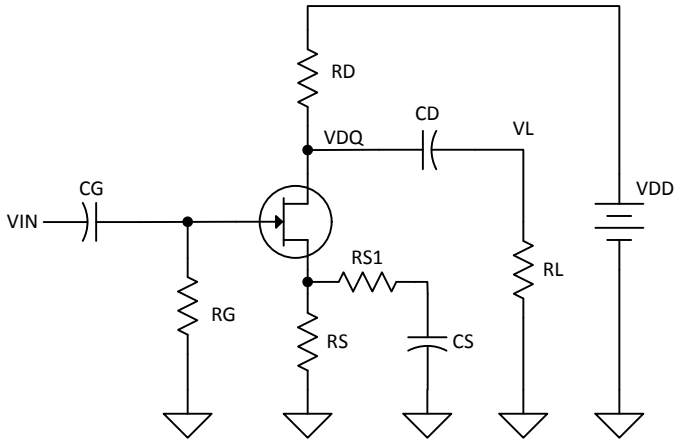
ID	VGS	VD	VG	VS	gm	Av	Avl	Pg (dB)
0.00142	-0.140	20.00	3.28	3.42	0.00375	0.900	0.596	28.782
0.00205	-1.642	20.00	3.28	4.92	0.00302	0.879	0.543	27.969
0.00334	-4.732	20.00	3.28	8.01	0.00204	0.831	0.445	26.252

JFET Homework

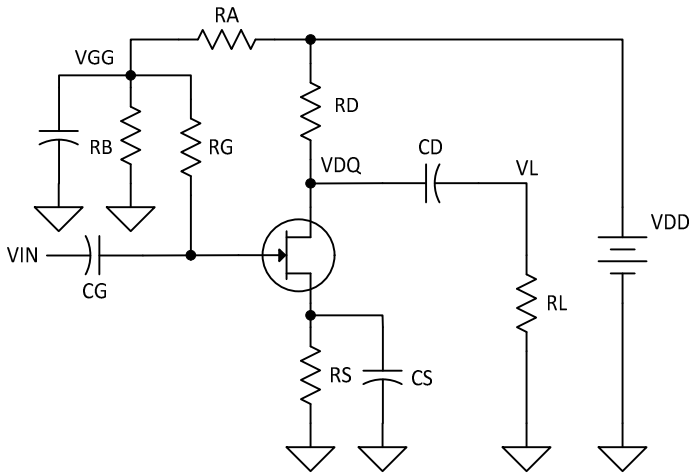
Design Problems

These problems are identical to problems 1 – 5 except approached from the design perspective – see problems 1-5 for the answers. The result is the designs you analyzed in the earlier problems. In all cases use the V_P data for the minimum I_{DSS}.

6. Complete the design of the following circuit. V_{DD} is +20 volts. The input resistance is to be 1 M. The drain current is to be 70% of I_{DSS}min. The load resistor is 470 Ohms and R_D is 680 Ohms. Av is to be -2.4 for a minimum I_{DSS} unit. Determine R_S and R_{S1}.

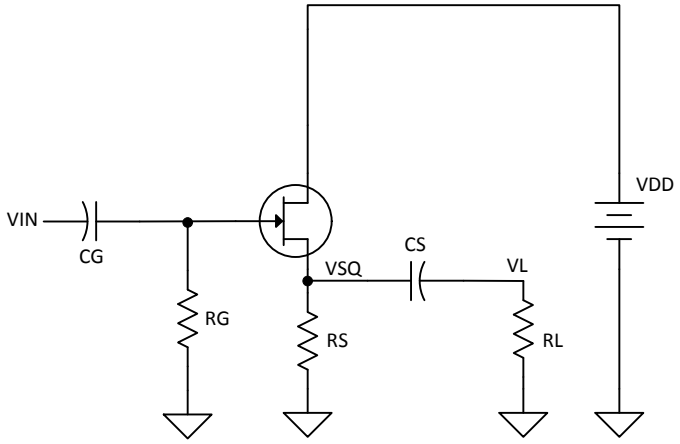


7. Complete the design of the following circuit. V_{DD} is +20 volts. The input resistance is to be 1 M. The drain current is to be 70% of I_{DSS}min. The load resistor is 470 Ohms, R^S is 1.8K and R_D is 680 Ohms. Av is to be -2.3 for a minimum I_{DSS} unit. Determine the required V_{GG} at the voltage divider formed by R_A and R_B (10K). Determine R_{S1} and R_A.

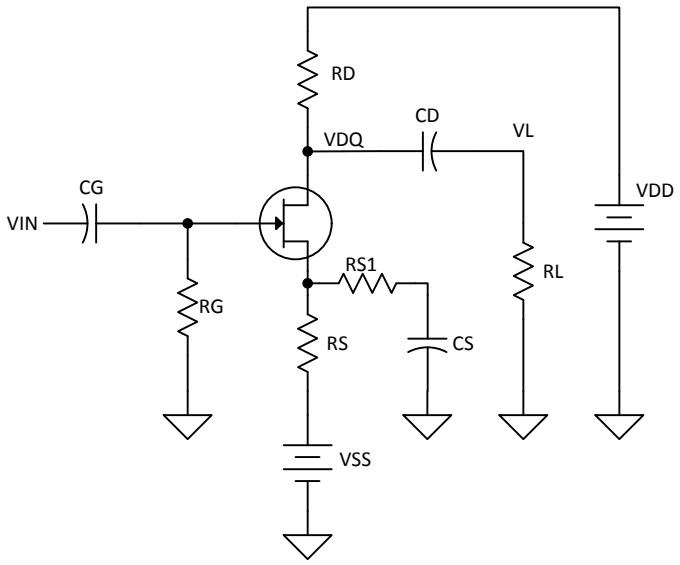


JFET Homework

8. Complete the design of the following circuit. V_{DD} is +20 volts. The input resistance is to be 1 M. The drain current is to be 70% of I_{DSS}min. The load resistor is 470 Ohms. Determine R_S. Remember that problem 3 is the analysis of this.



9. Complete the design of the following circuit. V_{DD} is +20 volts and V_{SS} is -2.5 volts. The input resistance is to be 1 M. The drain current is to be 70% of I_{DSS}min. The load resistor is 470 Ohms and R_D is 680 Ohms. V_S is to be close to as high as possible consistent with using an FET with the maximum V_P value (hint: reverse engineer problem 4 – think in terms of needing a V_{DS} of at least 8 volts). Av is to be -2.4 for a minimum I_{DSS} unit. Determine R_S and R_{S1}. Remember that problem 4 is an analysis of this.



JFET Homework

10. Complete the design of the following circuit. V_{DD} is +20 volts. The input resistance is to be 1 M. The drain current is to be 70% of I_{DSS}min. The load resistor is 470 Ohms. V_S is to be as high as possible consistent with using an FET with the maximum V_P value (hint: reverse engineer problem 5 – think in terms of needing a V_{DS} of at least 8 volts). Determine the required V_{GG} at the voltage divider formed by R_A and R_B (10K). Determine R_S and R_{S1} and R_A.