EE351 Laboratory Exercise 3
Transistor Amplifiers

Oct. 7, 2008

The purpose of this laboratory exercise is for the student to gain experience designing single stage transistor amplifiers using methods discussed in class. The student should come to lab with all designs worked out and checked via analytical methods and including a SPICE simulation of the DC operating points and AC gain analysis. The lab will confirm if the student has done the design correctly. This lab will be remarkably short for students who have done the proper designs and remarkably long otherwise.

Since some amount of judgment is used in the design process it is likely that there will be variations in the designs. There are a variety of component values that will satisfy the specifications. Each lab group (of two) should do the designs working together prior to lab – there may not be time in lab. The designs should be built and tested in lab and a group or individual report can be turned in.

Common Emitter Amplifier Design

The student is to design a common emitter amplifier to meet the following specifications. The amplifier will operate on a V_{CC} supply of 20 Volts and a V_{EE} supply of 0 Volts and should be designed for maximum possible linear output signal swing across a 3,300 Ohm load when driven by a 1,000 Hz sine wave signal source according to the Optimum V_{CQ} notes. Use 2.2 K for R_C and k=0.5 (for 5% distortion). Design for a loaded gain of 25. Design such that the ratio of the ratio of collector current at the maximum operating temperature of 60 degrees C divided by the minimum collector current at 0 degrees C is no more than 1.2. Design such that the ratio of collector current at a maximum beta of 240 divided by the collector current at a minimum beta of 80 is no more than 1.2. The design should be confirmed by analysis. Also analyze for the maximum peak-peak output signal at the specified distortion level. The basic circuit is in Figure 1.

Common Collector Amplifier Design

The student is to design a common collector amplifier to meet the following specifications. The amplifier will operate on a V_{CC} of 20 Volts and a V_{EE} supply of 0 Volts and should be designed for maximum possible linear output signal swing and produce an undistorted output of not less than 10 Vpp across a 1,000 Ohm load when driven by a 1,000 Hz sine wave signal source whose open circuit output voltage is 13 Vpp and whose source resistance is 2,000 Ohms. Design such that the ratio of the ratio of collector current at the maximum operating temperature of 60 degrees C divided by the minimum collector current at 0 degrees C is no more than 1.2. Design such that the ratio of collector current at a maximum beta of 240 divided by the collector current at a minimum beta of 80 is no more than 1.2. The design should be confirmed by analysis and the student should have calculations that predict the maximum possible undistorted loaded output signal level. The basic circuit is in Figure 2.

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Laboratory Work

1.0 Common Emitter Amplifier

1.1 Build your design for Figure 1.

1.2 Measure V_B, V_E, and V_C and confirm that these match your analysis within reason. If not then figure out why and make corrections before proceeding.

1.3 Adjust the input level such that the loaded output peak-peak level is as predicted in the design. Confirm that the distortion is visible but small. An alternate way to check this is to switch the signal source to a triangular wave as it is usually easier to spot deviations from a straight slope. If the output signal is obviously distorted then figure out what is wrong and make corrections before proceeding.

1.4 Now measure the loaded gain of the amplifier and verify that it matches the design specification. If not then make adjustments to R_{E1} to achieve this and then repeat step 1.3.

1.5 Measure the signal amplitude at the base of the transistor. Use this data in conjunction with the open circuit source voltage and source resistance to calculate the input resistance of the amplifier. Compare this to the calculated value from your analysis of the working design (either your original pre-lab analysis or your analysis of the corrected design if your design was faulty).

1.6 Continue increasing the amplitude of the signal source and observe the distortion effects on the output. Keep increasing up to about 5 Vpp at the signal generator output. Observe an interesting distortion effect when the positive peak signal at the base of the transistor becomes higher than the negative peak signal at the collector and the base-collector junction is forward biased and the collector signal voltage rises instead of falls – a polarity flip – in some systems this could be a critical or fatal fault.

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2.0 Common Collector Amplifier

2.1 Build your design for Figure 2.

2.2 Measure V_B and V_E and confirm that these match your analysis within reason. If not then figure out why and make corrections before proceeding.

2.3 Apply the specified signal and observe the loaded output signal on an oscilloscope and confirm that at most, only a small amount of distortion is visible. An alternate way to check this is to switch the signal source to a triangular wave as it is usually easier to spot deviations from a straight slope. If the output signal is obviously distorted then figure out what is wrong and make corrections before proceeding.

2.4 Now measure the output signal amplitude and confirm that it is within ten percent of the design value. If not then figure out what is wrong (input resistance is most likely too low) and make corrections before proceeding.

2.5 Measure the signal amplitude at the base of the transistor. Use this data in conjunction with the open circuit source voltage and source resistance to calculate the input resistance of the amplifier. Compare this to the calculated value from your analysis of the working design (either your original pre-lab analysis or your analysis of the corrected design if your design was faulty).

2.6 Increase the amplitude of the signal source while observing the amplifier output signal on an oscilloscope. Experimentally determine the maximum possible undistorted output signal. Compare this to your calculations.

2.7 Continue increasing the amplitude of the signal source and observe the distortion effects on the output. Keep increasing up to about 20 Vpp at the signal generator output. The output signal will become very clipped.

EE351 LAB 3 FIGURES

FIGURE 1

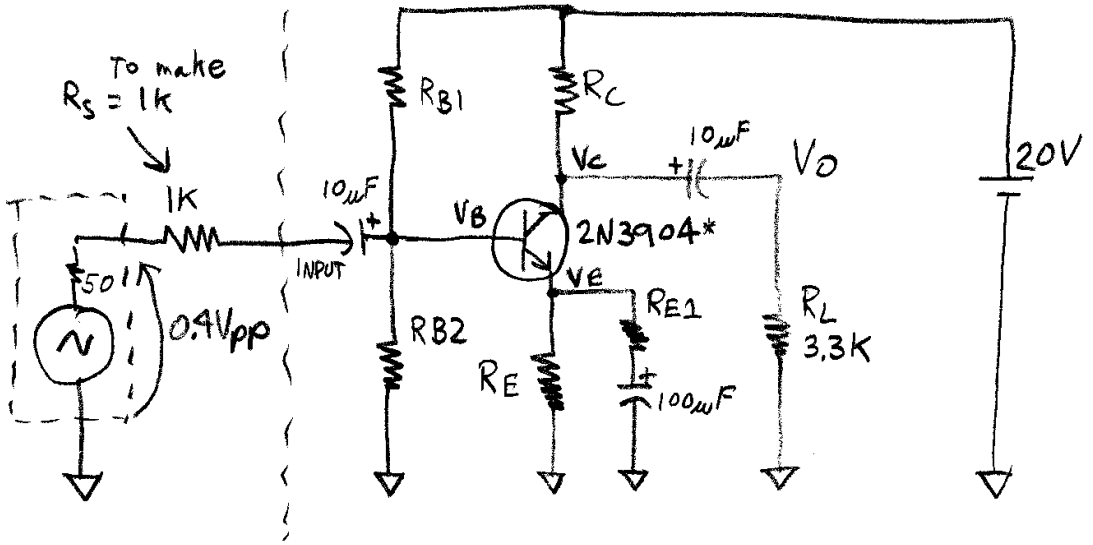
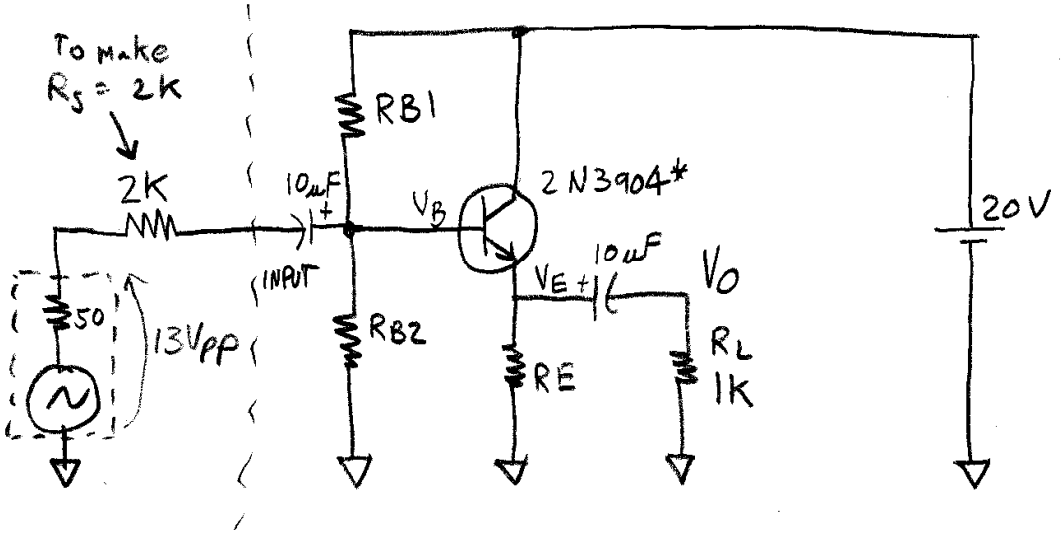


FIGURE 2



* OR OTHER NPN SUCH AS 2N2222A