# EE351 Laboratory Exercise 4
# Field Effect Transistors

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## Introduction

The purpose of this laboratory exercise is for students to gain experience making measurements on Junction Field Effect Transistors (JFET) to confirm mathematical models and to gain practical experience with analysis and design of JFET amplifiers. Do not use SPICE for this lab – the results will probably differ by a wide margin compared to your measured values. The only way to make SPICE work is to customize the JFET model to the IDSS and VP values you measure.

## 1.0 Initial Measurement and Setup

The first thing to do is to become familiar with your JFET and to verify that it is operational prior to doing experiments with it. Use the data sheet for your JFET to identify the gate, source, and drain leads. Since this is an N-channel JFET the gate is made of P-type semiconductor and the channel is made of N-type semiconductor.

For the following measurements, use an ohmmeter set on a range that can measure forward biased diodes (this is typically the 2K full-scale range – some meters have a special diode test range – use that if yours has one).

1.1 Confirm a forward bias condition when the plus lead is connected to the gate and the negative lead is connected to the source and then the drain.

1.2 Confirm a reverse bias condition when the negative lead is connected to the gate and the plus lead is connected to the source and then the drain.

1.3 Connect the ohmmeter across the drain and source (polarity does not matter) with the gate lead open and confirm some kind of conduction. JFETs vary widely so no specific value can be given here. Typically this can range from less than one hundred up to several hundred ohms. The key point is that if this measurement shows a high resistance (much over 1,000 ohms) then the JFET may be defective.

1.4 Continue to the next part if the JFET passed the above tests. Otherwise, try a different JFET.

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## 2.0 Measuring IDSS and VP

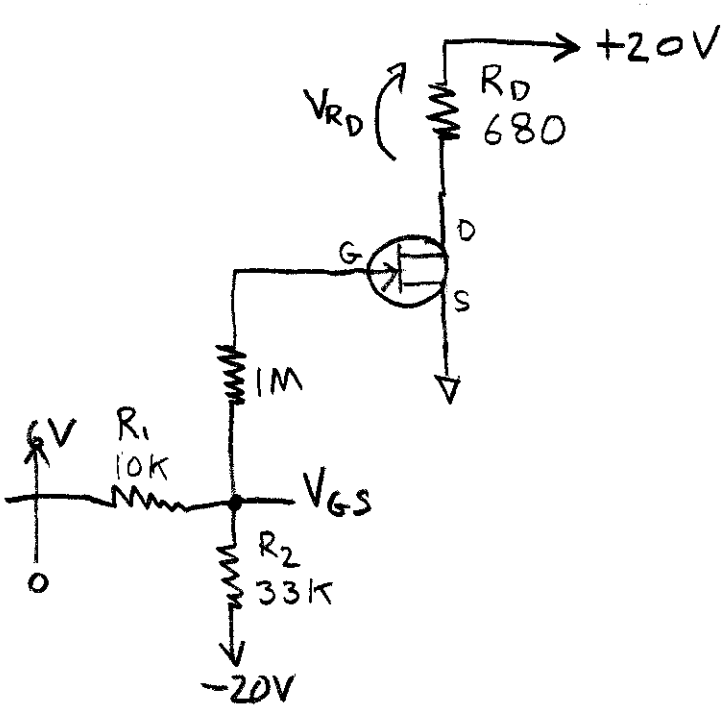


*Figure 1*

2.1 Build the circuit in Figure 1 but do not install the transistor yet. The 680 ohm drain resistor is about the largest that can be used if the IDSS of your JFET is at the high end of its possible range. The voltage divider network is designed to work with your lab power supply to convert the positive 0 – 6 volt control into a negative control for biasing the gate of the JFET. Verify that the gate voltage varies from about -4.6 to 0.0 as the 0 – 6 volt supply is varied from 0 to 6 volts. Fix any problems before continuing.

2.2 Install the transistor and set the gate voltage to 0.00 volts. Measure the voltage, VRD, across RD and compute the drain current from Ohm's law – this is the method to use for measuring drain current in subsequent steps. Record this current as IDSS. This should be between about 2 and 20 mA. Use a different JFET if this current is more than 20 mA.

2.3 Adjust the gate voltage to -4.6 volts and measure and record the drain current. It should be significantly smaller than IDSS and may be zero depending on your particular JFET. If not then there is something wrong – either you have a wiring error or the JFET is defective. Do not proceed until whatever problem is fixed.

2.4.0 Measuring VP is a bit tricky as it can be difficult to define a point at which ID just reaches zero – actually a very small residual current. This can cause the magnitude of VP to be overstated. To make it easier for the student to obtain

credible results for this lab the measurement will be made at a specific point and extrapolated to VP. Using the standard mathematical model for a JFET, the student should show that when (ID/IDSS) = 0.01 that (VGS/VP) is 0.9. Thus, we adjust VGS so that the drain current is one percent of IDSS and then divide that voltage by 0.9 to obtain a good value for VP.

2.4.1 Adjust the gate voltage such that the drain current, ID, is one percent of the measured IDSS. If, for your particular JFET, you need to go below -4.6 volts for the gate voltage then change the 33K resistor in the voltage divider network to 15K. This will permit a gate voltage adjustment range of -8 to -4.4 volts. It should not take more than -8 volts to bring ID to near zero. Start over with another FET if this does not work.

2.4.2 Divide the gate voltage from 2.4.1 by 0.9 to obtain a good value for VP. Record this value. You now have the basic model information for your JFET.

## 3.0 Plotting transfer characteristics

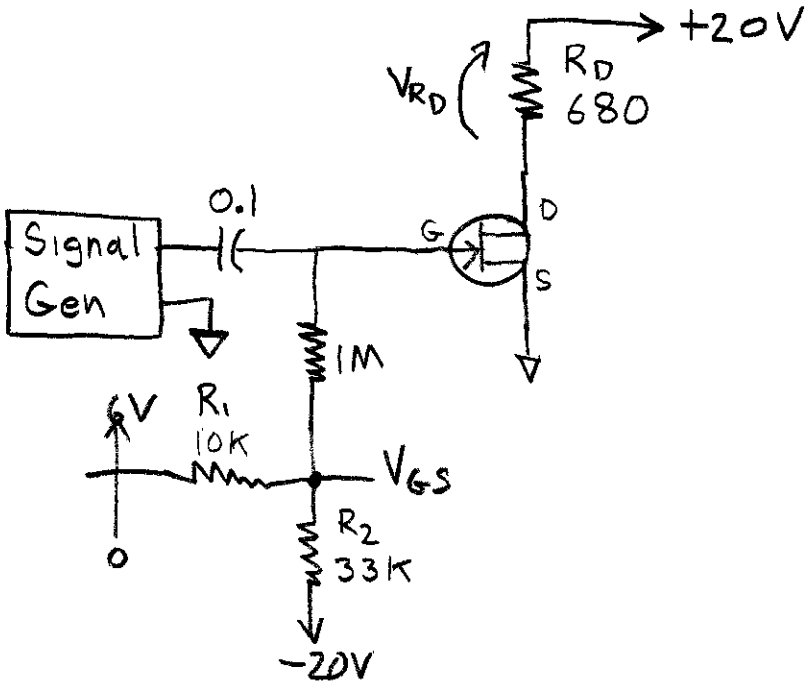


*Figure 2*

The student will plot the ID versus VGS and gm versus VGS over the range of VGS from VP to 0. Connect the circuit in Figure 2. Depending on your particular JFET you may need to start with R1 = 33K and then change to R2 = 15K if more than -4.6 volts is needed. Note that ID is the DC voltage across RD divided by RD.

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The 1000 Hz sine wave signal generator provides a varying gate voltage so that the resulting variation in ID can be measured. This permits the gm to be calculated for each operating point. A low value of 0.1 Vpp is used for the vgs so that the system is linear. Note that id is the peak-peak voltage measured (using a scope) at the drain terminal and then divided by RD (the other end of RD is at signal ground) and that gm is id/vgs. Expect ratios in the 0.003 range for VGS = 0 down to below 0.0001 for VGS approaching VP.

3.1 Complete the following table. There is no point taking data beyond VP.

| **VGS** | **ID** | **id** |
|---|---|---|
| 0.0 V | _____ mA | _____ mApp |
| -0.2 | _____ | _____ |
| -0.4 | _____ | _____ |
| -0.6 | _____ | _____ |
| -1.0 | _____ | _____ |
| -1.2 | _____ | _____ |
| -1.4 | _____ | _____ |
| -1.6 | _____ | _____ |
| -1.8 | _____ | _____ |
| -2.0 | _____ | _____ |
| -2.2 | _____ | _____ |
| -2.4 | _____ | _____ |
| -2.6 | _____ | _____ |
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| -4.4 | _____ | _____ |
| -4.6 | _____ | _____ |
| -4.8 | _____ | _____ |
| -5.0 | _____ | _____ |
| -5.2 | _____ | _____ |
| -5.4 | _____ | _____ |
| -5.6 | _____ | _____ |
| -5.8 | _____ | _____ |
| -6.0 | _____ | _____ |

Continue if needed until VP is reached for your particular JFET.

3.2 Plot the actual ID versus VGS data from data in 3.1 and the theoretical data from the model of your JFET together.

3.3 Plot the actual gm versus VGS data from data in 3.1 and the theoretical data from the model of your JFET together. Also plot (on a different graph) the actual gm versus ID data from data in 3.1 and the theoretical data from the model of your JFET together.

## 4.0 Common Source Amplifier

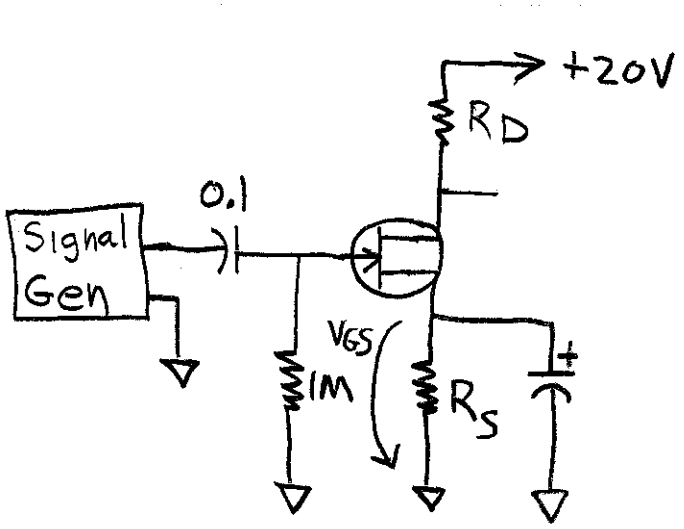


*Figure 3*

4.1 Build the circuit in Figure 3. To customize this part of the lab for good results for your particular JFET, choose a convenient value of RD that is around 20/IDSS – this is only a rough guideline. Calculate the required value of RS to bias the JFET for an ID that is half of IDSS. Use the nearest standard resistor.

4.2 Measure VD and compute the actual ID. Compare these to the predicted values from analysis. Hint: VD should be in the general vicinity of 10 volts –give or take about 3 volts. Figure out what is wrong if this is not the case – otherwise the next part of the lab will not work right.

4.3 Adjust the signal generator output level to a 0.1 Vpp 1000 Hz sine wave as measured at the gate terminal of the FET. Measure the peak-peak AC signal amplitude at the drain terminal. Compute the actual gain and compare to the theoretical gain calculation. Use the gm you measured for the actual drain current you are using.

4.4 Connect a load resistor (between about half and twice the value you are using for RD) as shown in Figure 4. Measure the AC voltage across the load. Compute the actual gain and compare to the theoretical gain calculation. Using the voltage divider equation, compute the output resistance of the amplifier and compare with the theoretical value. Compute the power gain of the amplifier.

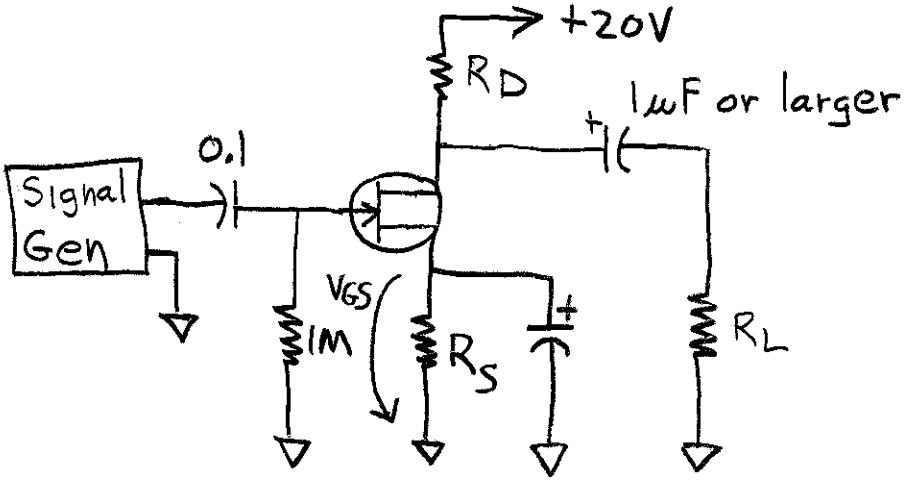


*Figure 4*

4.5 Increase the amplitude from the signal generator until some kind of distortion is observed in the waveform across the load resistor. Usually the first visible sign of distortion is non-symmetrical halves of the sine wave across the load. Record the peak-peak output amplitude obtained.

4.6 Increase the amplitude from the signal generator until on half of the sine wave across the load begins to clip and observe the distortion.

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## 5.0 Common Drain Amplifier

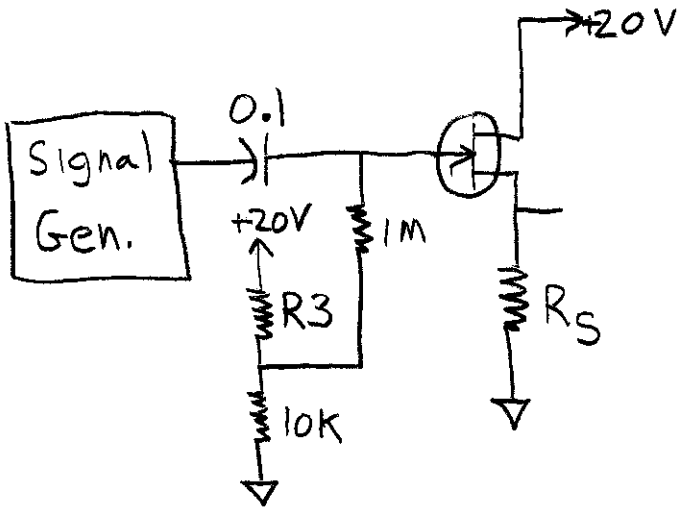


*Figure 5:Common drain amplifier*

5.1 Complete the design of the circuit in Figure 5. Use the same resistor for RS as you used for RD in the previous part. Calculate the value of R3 to bias the JFET for a drain current three fourths of IDSS. Remember that you know VS from the product of ID and RS and that you need a specific VG to form the required VGS for the target drain current. Complete the design of the voltage divider to obtain that VG.

5.2 Build the circuit in Figure 5 and measure VS and VG. From these values, compute ID and VGS. Check these against the values calculated from analysis using the model of your JFET.

5.3 Apply a 0.1 Vpp 1000 Hz sine wave signal as measured on the gate terminal and measure the peak-peak signal at the source terminal. Compute the voltage gain of the amplifier and compare with the value from analysis.

5.4 Refer to Figure 6 and connect the same load resistor as used in the previous part and measure the peak-peak signal across it. Compute the voltage gain of the amplifier and compare with the value from analysis. Using the voltage divider equation, compute the output resistance of the amplifier and compare with the theoretical value. Compute the power gain of the amplifier.

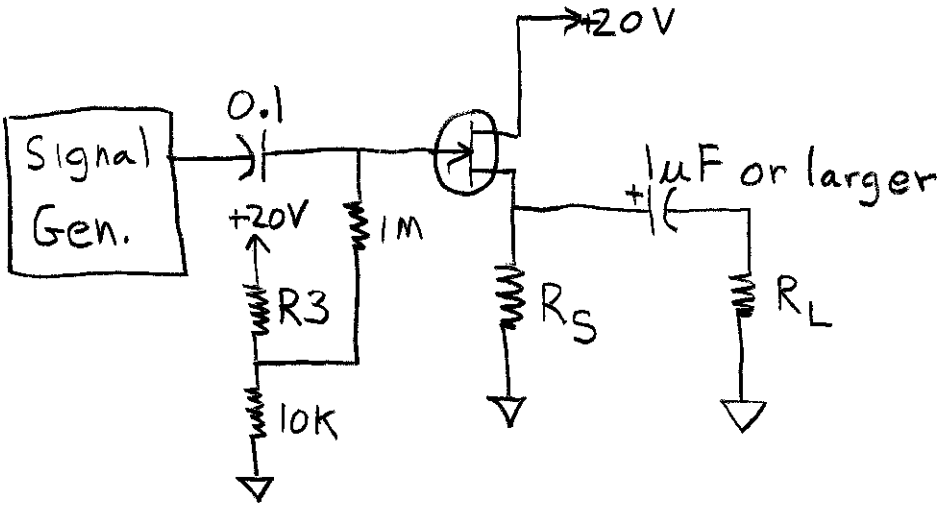


*Figure 6*

5.5 Increase the amplitude from the signal generator until some kind of distortion is observed in the waveform across the load resistor. Usually the first visible sign of distortion is non-symmetric halves of the sine wave across the load. Record the peak-peak output amplitude obtained.

5.6 Increase the amplitude from the signal generator until on half of the sine wave across the load begins to clip and observe the distortion.