

Multistage Amplifiers

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Introduction

There is a limit to how much gain can be achieved from a single stage amplifier. Single stage amplifiers also have limits on input and output impedance. Multistage amplifiers are used to achieve higher voltage gain and to provide better control of input and output impedances. Two significant advantages that multistage amplifiers have over single stage amplifiers are flexibility in input and output impedance and much higher gain. Multistage amplifiers can be divided into two general classes, open-loop and negative feedback. Open-loop amplifiers are easy to understand but are sensitive to environment and component variations and difficult to design for accuracy. Negative feedback amplifiers are a bit more difficult to understand but have the advantage of being much less sensitive to environment and component variations and also enable better control of input impedance, closed-loop gain, and output impedance. The fundamental building block of a negative feedback amplifier is a high voltage gain multistage open-loop amplifier known as an operational amplifier.

Multistage structures

We will begin by examining all possible two-stage amplifiers using some combination of common-emitter and common-collector stages. This forms the fundamental building blocks for any number of stages.

The use of capacitor coupling between stages requires a lot of capacitors and resistors that could be eliminated with innovative design. The key to this is to arrange for the quiescent voltage at the output of one stage to be the same as the desired quiescent voltage at the input of the next stage. Then the AC coupling capacitor and associated bias resistors are not needed. Good designs use all the parts that are needed but no more.

NPN and PNP transistors are often used in multistage amplifiers for improved characteristics over what could be achieved by using only one transistor type. Temperature sensitivity can be greatly reduced using both types in certain circuits such that the base-emitter voltage drops practically cancel – thus greatly reducing the effect of temperature. Each individual voltage drop is very temperature sensitive but the net result is the subtraction of the two. Use of an NPN common-emitter stage followed by a PNP common-collector stage (or vice-versa) for the output enables near optimum bias conditions for both.

Common-emitter – common-emitter

The structure shown in Figure 1 is used when the voltage gain needs to be high. Voltage gains from several hundred to several thousand are possible.

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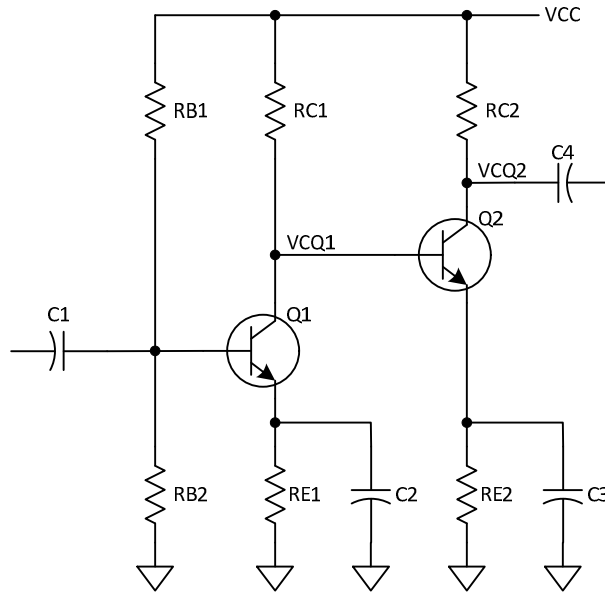


Figure 1: Example of multistage amplifier using two common-emitter stages

Common-emitter – common-collector

The structure in Figure 2 is used to significantly lower the output impedance of a standard common-emitter amplifier.

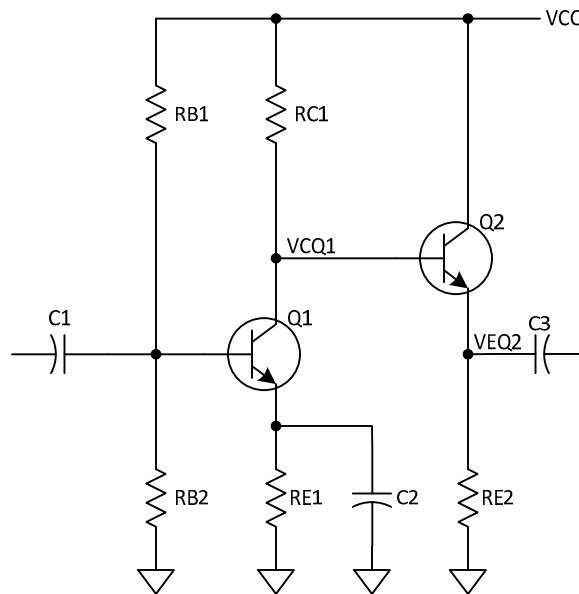


Figure 2: Example of common-emitter followed by common collector

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Common-collector – common-emitter

The structure in Figure 3 is used to significantly raise the input impedance of a common-emitter amplifier. Observe that the structure on the right utilizes a PNP transistor for the input and an NPN transistor for the common-emitter amplifier. The result is that the temperature dependent base-emitter voltages practically cancel resulting in a very temperature stable design.

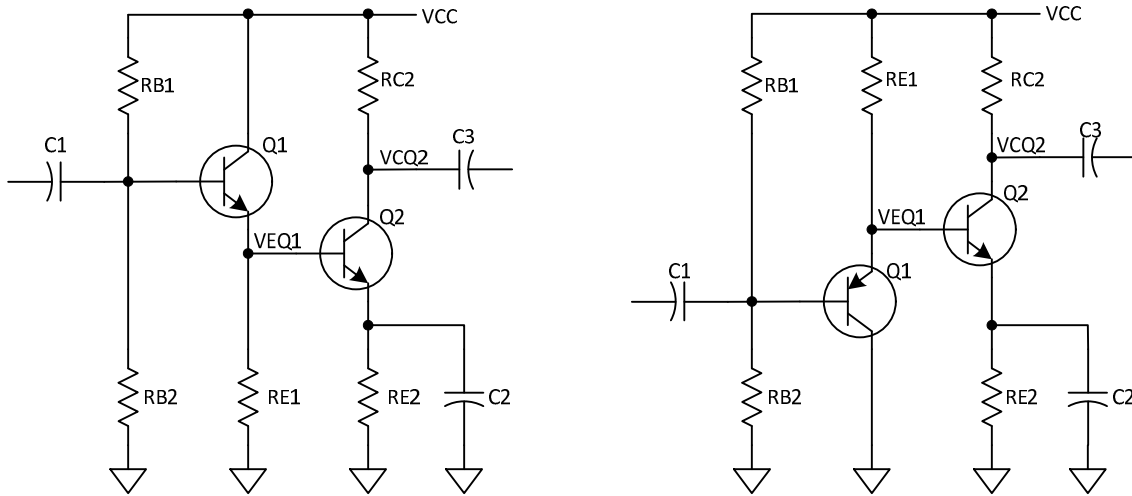


Figure 3: Examples of common-collector followed by common-emitter

Common-collector – common-collector

This structure with a voltage gain less than 1 (but current gain in the hundreds) is used to achieve higher input resistance and lower output resistance than can be achieved in a single common-collector stage. The structure on the right achieves temperature insensitivity by using a PNP-NPN combination.

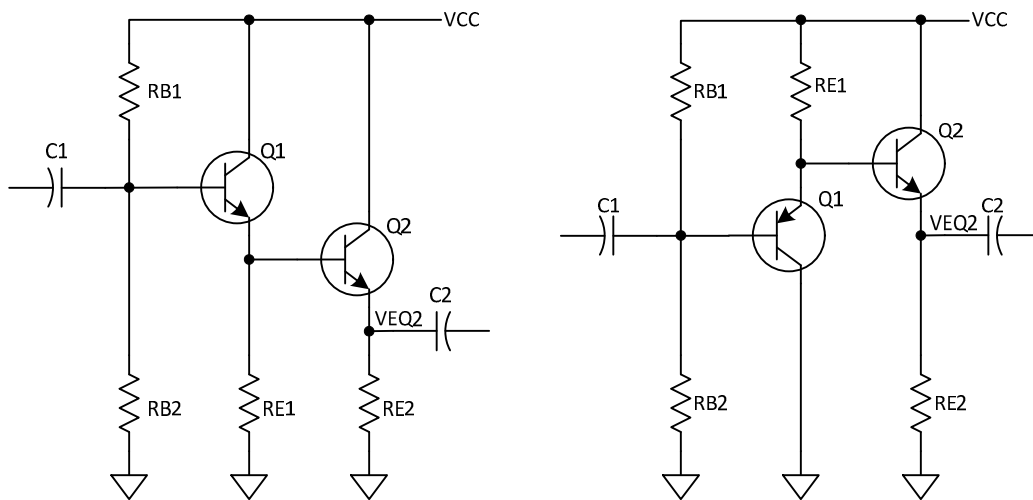


Figure 4: Examples of two stages of common-collector

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The above forms can be extended to higher number of stages. The final example is a three stage amplifier with the structure common-collector, common-emitter, common-collector. This structure achieves high input impedance, high voltage gain, and low output impedance. The use of PNP and NPN transistors on the input virtually cancels the effects of temperature on bias stability.

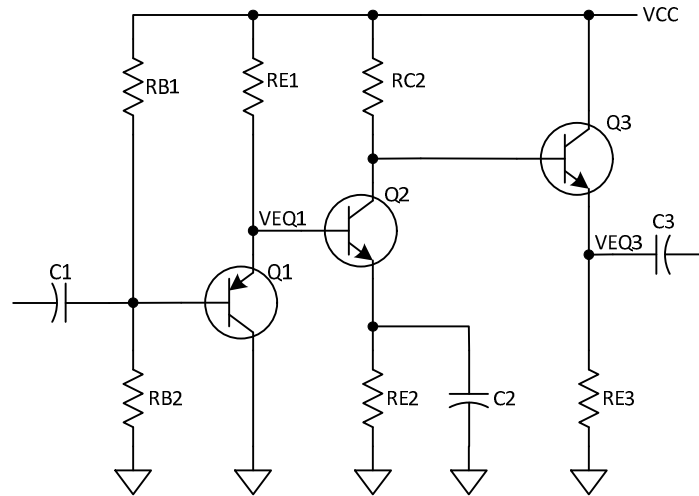


Figure 5: Three stages – common-collector, common-emitter, common-collector

General Characteristics of Typical Multistage Amplifier Structures

Stage Number				Characteristics		
1	2	3	4	R _{in}	R _{out}	Voltage gain
CE	CE			Medium	Medium	High
CE	CC			Medium	Low	Medium
CC	CE			High	Medium	Medium
CC	CC			Very high	Very low	<1
CE	CE	CE		Medium	Medium	Extremely high
CE	CE	CC		Medium	Low	Very high
CE	CC	CE		Medium	Medium	Very high
CE	CC	CC		Medium	Very low	Medium
CC	CE	CE		High	Medium	Very high
CC	CE	CC		High	Low	Medium
CC	CC	CE		Very high	Medium	Medium
CC	CC	CC		Very high	Very low	<1
CC	CE	CE	CC	High	Low	Very high

Descriptor	R _{in} or R _{out}	Voltage gain
Low	Less than a few hundred Ohms	
Medium	A few hundred to a few thousand Ohms	Less than 50
High	A few thousand to a few ten thousand Ohms	50 to 500
Very high	Many tens of thousands of Ohms	500 to 5000
Extremely high	Over one hundred thousand Ohms	Over 5,000

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Analysis of multistage amplifiers

Analysis of multistage amplifiers is performed stage at a time starting with the input stage and progressing to the output stage using identical methods for single stage amplifiers. One point of confusion for students analyzing direct coupled amplifiers is that the collector resistor for one stage becomes the base resistor for the next stage. In stages involving common-collector amplifiers some modified approaches, including some simplifying approximations, are necessary because characteristics of common-collector stages are dependent on external impedances. The student should not be afraid of approximations since that is routinely done all the time in the profession. Even the seemingly precise methods learned so far in the course for single stage amplifiers are actually approximations.

The first step in analysis is to break the multistage circuit into individual stages and perform DC analysis first and then followed by AC analysis. This means that the connection to the transistor base of stage 2 is temporarily opened. The first stage is then a standard single stage amplifier with standard single stage analysis. For all of the examples in Figures 1 through 4 we would first find V_{BB} and R_B as we always have and then calculate the emitter and collector currents and the values of V_{CQ} or V_{EQ} – unloaded since the next stage is not yet connected.

Bias analysis of the second stage uses the results of bias analysis of the first stage. We arrive at the V_{BB} and R_B to use for the second stage via a different method than used for single stage analysis.

If the first stage was a common-emitter amplifier then the V_{BB} to use for stage 2 is V_{CQ1} and R_B is R_{C1} . This is the Thévenin equivalent as we have always used. One thing to keep in mind is that the actual value of V_{CQ1} will be a bit lower since the calculated value was based on no load. That is normal – note that in our standard single stage analysis that the magnitude of V_{BQ} is a little bit lower than V_{BB} because of voltage drop across R_B . The single stage math developed takes that into account. We need the unloaded Thévenin value to compute I_E for the second stage as we did using V_{BB} for the first stage.

If the first stage was a common-collector amplifier then the V_{BB} to use for stage 2 is V_{EQ1} and R_B is taken to be zero (in reality the true magnitude of R_B is perhaps as high as several tens of ohms – and can be a challenge to accurately determine – but looking at the equation for computing I_E for the second stage, it will make miniscule difference if R_B is zero or 50 ohms – so make life easy and use zero.

We perform input impedance analysis the same way as for single stage amplifiers except that if the first stage is common-collector we will have to factor in the input impedance of the next stage just like we factored in the load impedance for a single stage common-collector amplifier.

We perform output impedance analysis the same was as for single stage amplifiers. If the output stage is common-collector then we use the output impedance of the previous stage for the $R_B || R_S$ term in the equation – just like we did for single stage amplifiers.

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Gain analysis is also performed the same way – analyzing each stage using the same single stage methods we already know. Then the composite gain is found using the generic cascaded amplifiers mathematics early in the course.

Design of multistage amplifiers

The design of multistage amplifiers begins at the output and progresses backwards to the input. Initially the number of stages is not known. The design progresses with additional stages until the requirements are met. It is common for there to be a lot of iteration in the design and the number of stages might vary with each iteration because initially it is not known how many stages will be needed. There are some differences in the approach to the design of multistage amplifiers compared to techniques learned for single stage amplifiers although the process is very similar. A key difference is that generally we only have to be concerned with large signals in the output stage. Design of multistage amplifiers is not part of this course.

Operational amplifiers

While there are many different multistage structures used for various special case applications, there is one generic structure that is very useful for a broad class of applications. This structure is known as an operational amplifier (commonly abbreviated op-amp) because depending on the external components the amplifier is capable of performing a variety of mathematical operations such as scaling (i.e. basic amplification), addition, subtraction, integration, differentiation. Using non-linear components in the feedback network it is possible to perform absolute value, computing the logarithm or exponent of an input voltage or current, and perform limiting or hysteresis functions. All of these seemingly complicated functions are remarkably easy to accomplish using an operational amplifier as the fundamental building block. Early operational amplifiers were used as building blocks for analog computers – that is where the name, operational, came from.

An op-amp is comprised of three fundamental amplifier stage groups although the actual number of stages might be a few more.

1. **Differential amplifier input stage:** Rather than amplifying a single input signal, this stage amplifies the difference between two input signals.
2. **High voltage gain stage:** This is a common-emitter amplifier.
3. **Low output impedance stage:** This is a common-collector amplifier with voltage gain a little less than unity but high current gain.

The overall voltage gain of the three amplifiers is typically several thousand as a minimum and can be over one million in some advanced integrated circuits. Figure 6 illustrates the simplest

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possible operational amplifier having all three of the above characteristics. The individual stages are separated by dotted lines for clarity.

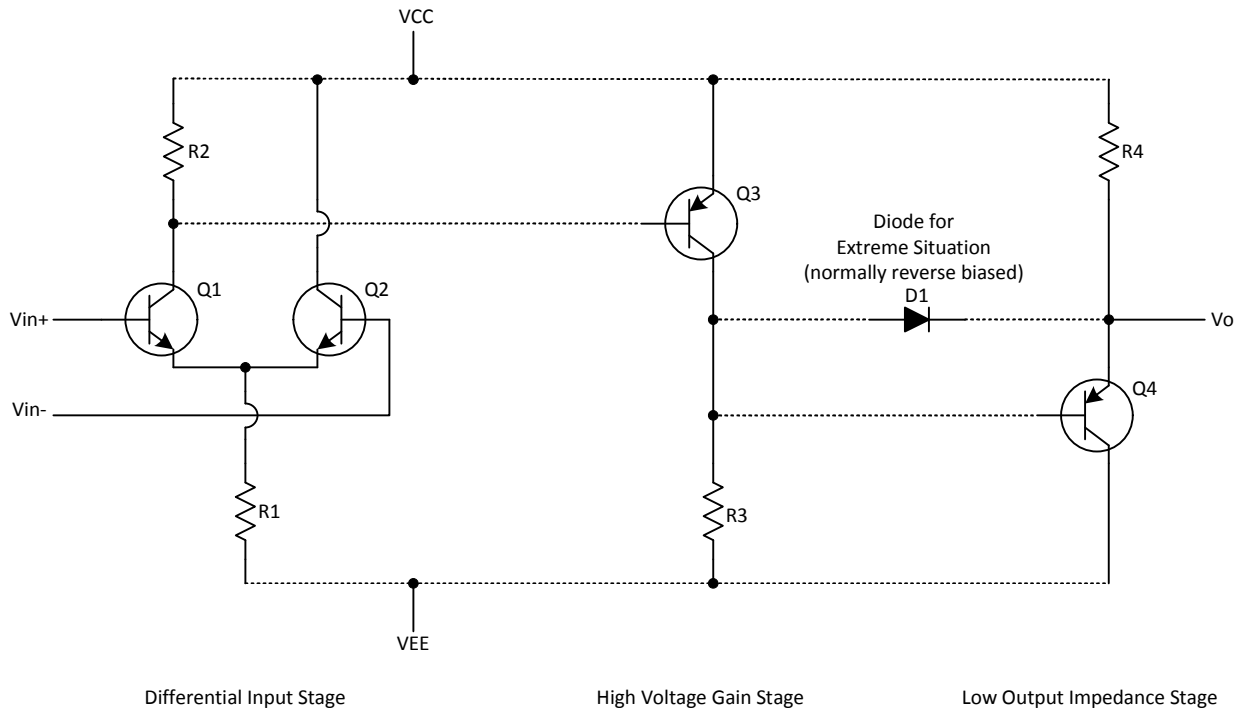


Figure 6: Simplest possible operational amplifier

Analysis of a simple op-amp

Op-amps are intended to be used with negative feedback as the closed-loop applications make the circuit so useful. For analysis we first consider the open-loop case and then apply the results of that to the closed-loop case. However, we have a problem – it is not possible to analyze a multistage high gain direct coupled amplifier in open-loop because small approximation errors are highly magnified by the high gain and will mathematically render the circuit as non-operational even though the circuit may work very well in closed-loop application. Our solution is to analyze the amplifier using assumptions that will become very accurate for the closed-loop situation. This approach is not intuitively obvious at first but becomes clear as one gains experience with op-amps. This is the beauty of closed-loop amplifiers with negative feedback – errors are highly reduced.

For the analysis, we will use the laboratory version of the Figure 6 circuit that students will build with $V_{CC} = +15$ volts, $V_{EE} = -15$ volts, $R_1 = 100K$, $R_2 = 10K$, $R_3 = 62K$, and $R_4 = 3.6K$. We will assume all transistors have a beta of 150 and that all transistors have a V_{BE} of 0.62 volts. We will use 0.026 volts for the thermal voltage.

We start with the differential input stage consisting of Q_1 and Q_2 . We will assume that V_{in+} and V_{in-} are both at zero volts. For many of the example circuits this will actually be the case

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once the feedback loop is closed. We compute the current through R1 as $(0 - 0.62 - -15)/100K = \underline{144 \text{ uA}}$. This current will split between the emitters of Q1 and Q2. There is no way to know exactly how the split will end up but the best guess is to assume equal split – it is not really important anyway. Thus, each transistor will conduct $\underline{72 \text{ uA}}$. The r_e looking into the emitter of each transistor is $0.026/72 \text{ uA} = \underline{362 \text{ ohms}}$. Q1 is a common-emitter amplifier for V_{in+} . Its gain is $-(150/151) * 10,000 / (362+362) = \underline{-13.7}$. Note that the r_e of Q2 is in series with the emitter circuit of Q1. The effect of R1 (100K) is ignored for simplicity since its effect is tiny.

Q2 and Q1 form a two-stage amplifier for V_{in-} . Q2 is a common-collector amplifier for V_{in0-} . Q1 is a common-base amplifier for the output of Q2. The loaded (remember that r_{e1} is the load) gain of Q2 is $r_{e1}/(r_{e1} + r_{e2}) = \underline{0.5}$. The voltage gain of Q1 is $(150/151) * 10,000 / 362 = \underline{13.7}$. This is the same magnitude as the gain for V_{in+} . Thus, the signal at the collector of Q1 is $(V_{in-} - V_{in+}) * 13.7$. This means that the difference between the two input voltages is amplified rather than just the input voltage. That is a very powerful function that makes op-amps so useful.

Normally, analysis would continue with the next stage but we need to use the bias conditions that will exist when the external feedback loop is closed. So, we start with the output of the amplifier at the emitter of Q4 and assume that it is at zero volts (that assumption will be very accurate later). We determine the emitter current of Q4 as $(15 - 0) / 3.6K = \underline{4.2 \text{ mA}}$. The dynamic resistance, r_{e4} , is then $0.026 / 4.2 \text{ mA} = 6.2 \text{ ohms}$. The resistance looking into the base of Q4 is $151 * (6.2 + 3,600) = \underline{544K}$. The voltage gain of the common-collector amplifier, Q4, is $3,600 / (6.2 + 3,600) = \underline{0.988}$.

The voltage at the base of Q4 is $0 - 0.62 = \underline{-0.62 \text{ volts}}$. The current through R3 is $(-0.62 - -15) / 62,000 = \underline{232 \text{ uA}}$. The base current of Q4 is $4.2 \text{ mA} / 151 = \underline{27.6 \text{ uA}}$. Thus, the collector current of Q3 is $232 \text{ uA} - 27.6 \text{ uA} = \underline{204.3 \text{ uA}}$. The emitter current of Q3 is then $(151/150)*204.3 \text{ uA} = \underline{205.7 \text{ uA}}$. The dynamic emitter resistance, r_{e3} , is $0.026/205.7 \text{ uA} = \underline{126.4 \text{ ohms}}$. The input resistance at the base of Q3 is $151 * 126.4 = \underline{19,100 \text{ ohms}}$. The unloaded voltage gain of the common-emitter amplifier, Q3, is $-(150/151)*62,000 / 126.4 = \underline{-487.3}$.

The voltage division between the output of the differential input stage and the high voltage gain stage is $19,100 / (10,000 + 19,100) = \underline{0.656}$. The voltage division between the output of the high voltage gain stage and the low output impedance stage is $544,000 / (62,000 + 54,000) = \underline{0.898}$.

We now can compute the voltage gain of the entire amplifier as $-13.7 * 0.656 * -487.3 * 0.898 * 0.988 = \underline{3,936}$. That is a lot of gain. This is a simple amplifier. With some advancements, that gain can easily be increased by a factor of ten and even a further factor of ten. In practice, we do not care what the actual gain of the amplifier is provided it is a large number such as this example. In the examples that follow it would make very little difference if the gain were 3,000 or 5,000.

The purpose of diode, D1, in the circuit is to prevent substantial reverse voltage across the base-emitter junction of Q4 for the nonlinear situation where the output voltage is forced to be low (think low-impedance) and Q3 is attempting to drive the output positive. For that situation the base-emitter junction of Q4 is reversed biased. Ordinarily, reverse bias of a PN junction is not an issue provided current is limited (i.e. power dissipation is limited) if breakdown occurs. For

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BJTs reverse base-emitter bias voltages higher than around 4 or 5 can cause permanent damage to the transistor even if there is no significant heating. D1 limits the reverse bias to approximately 0.65 volts which is safe.

Standard symbol and application examples

Although the internal structures vary a lot between the many various commercial integrated circuit op-amps, the basic function is identical. Therefore we use a schematic symbol to represent the op-amp as shown in Figure 7.

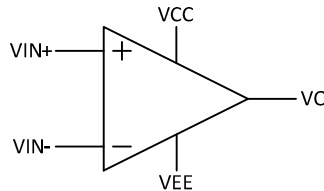


Figure 7: Standard schematic symbol for an op-amp
This symbol represents the circuit in Figure 6

The detailed mathematics of the following common operational amplifier circuits will be covered in EE431. For now, observe how simple it is to use operational amplifiers to build complex functions. Several of these circuits will be illustrated in the corresponding laboratory exercise using the op-amp in Figure 6. Think about how challenging it would be to design individual transistor circuits to accomplish the example functions. The nice thing about an op-amp is that we only have to design one generic amplifier that we can use for a wide variety of applications. Note that the circuits have no AC coupling capacitors and work even for DC input voltages.

In all of the following examples the output of the amplifier is the result of a huge gain on the voltage difference between the two inputs. With negative feedback to the inverting input (VIN-) then that input is driven towards matching the voltage at the non-inverting input (VIN+). Thus, the two input voltages are always practically equal. The inverting input “follows” the non-inverting input.

Non-inverting amplifier

In Figure 8 the VIN- input is from a voltage divider on VO, $V_{IN-} = VO \cdot R_1 / (R_1 + R_2)$ and $VO = (V_{IN+} - V_{IN-}) \cdot A_v$. Substituting the first equation into the second and with a little algebra we have:

$$V_o = \frac{V_{in} \left(1 + \frac{R_2}{R_1}\right)}{\frac{1 + \frac{R_2}{R_1}}{A_v} + 1} \quad (1)$$

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We see that if A_v is large in comparison to the term, $1 + R_2/R_1$ then the denominator is practically 1 and all we need be concerned with is the numerator. This is why we don't concern ourselves with the actual value of the open loop gain, A_v . As long as A_v is sufficiently large it has little effect on our result. The math for all of the circuits in the following examples is very similar.

So, for the circuit in Figure 8, $V_O = V_{IN} * (1 + R_2/R_1)$. Note how simple it is to set the desired gain – a simple resistor ratio. For example, if R_1 is 100 ohms and R_2 is 10,000 ohms then $V_O = 101 * V_{IN}$. The complications of designing an amplifier with a gain of 101 using earlier single stage methods are eliminated.

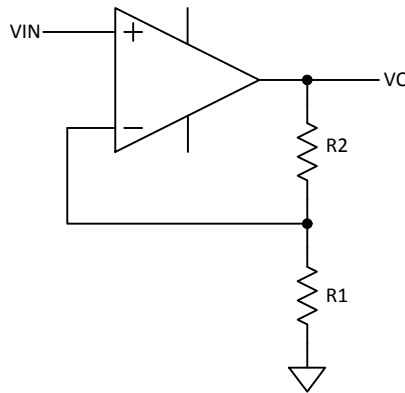


Figure 8: Non-inverting op-amp circuit

Inverting amplifier

In Figure 9, $V_O = -V_{IN} * (R_2/R_1)$. Again, note how simple it is to set the desired gain. The negative sign on the transfer function means that the output waveform is inverted from the input. For example, if R_1 is 1,000 ohms and R_2 is 100,000 ohms then $V_O = -100 * V_{IN}$.

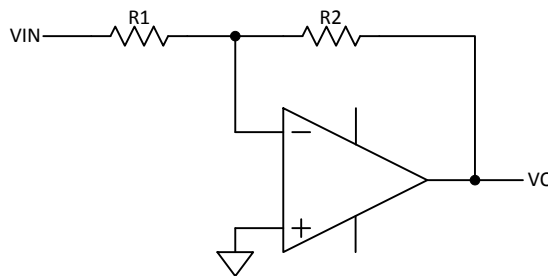


Figure 9: Inverting op-amp circuit

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Inverting Summer

In Figure 10, $V_O = -[VIN1*(R3/R1) + VIN2*(R3/R2)]$. This concept can be extended for practically an unlimited number of inputs. The resistor ratios can be set to 1.00 for simple summation or to any ratio for different scale factors on each input. For example, if R1 is 10K, R2 is 5K and R3 is 20K, then $V_O = -2*VIN1 - 4*VIN2$.

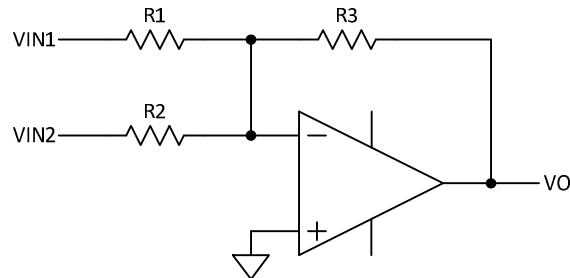


Figure 10: Inverting op-amp adder circuit

Subtractor circuit

In Figure 11, if all resistors are the same value then $V_O = (VIN1 - VIN2)$. It is possible to achieve various scale factors on the subtraction or different scale factors on each term with different value resistors. An example transfer function is $V_O = K1*VIN1 - K2*VIN2$.

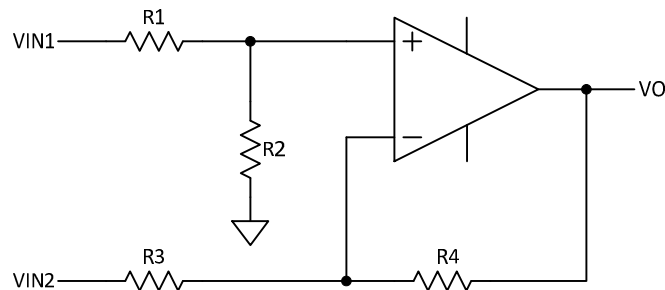


Figure 11: Subtractor circuit

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Integrator circuit

In Figure 12, $V_O(s) = -V_{IN}(s)/R_1C_1$. The negative sign because the inverting structure is used. Observe that the scale factor on the integration is $1/R_1C_1$. Integrators are often used in control circuits.

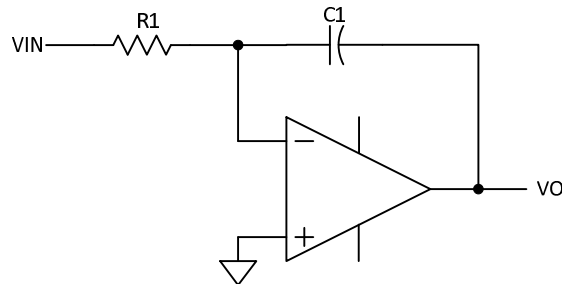


Figure 12: Integrator circuit

Differentiator circuit

In Figure 13, $V_O(s) = -R_1C_1 * V_{in}(s)$. If the input is a sine wave then the output is a cosine wave. If the input is a triangle wave then the output is a square wave since the derivative of a constant change in voltage is a fixed voltage.

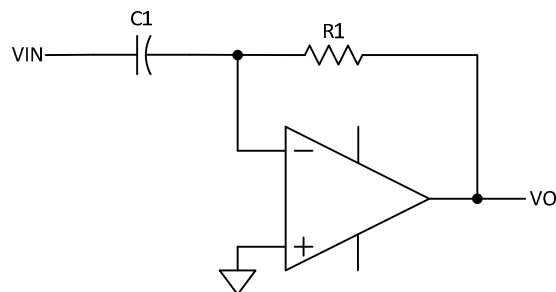


Figure 13: Differentiator circuit

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Precision half-wave rectifier

The circuit in Figure 14 uses the rectifier diode (D2) in the feedback of the op-amp which results in the non-linearity of the diode being reduced by the gain of the amplifier. Thus, small signals in the millivolt range can be accurately rectified. Diode, D1, provides a finite feedback path when the signal is of the opposite polarity. Thus, the voltage at the inverting input of U1 is held at zero volts and the voltage across R2 is the half-wave version of the input signal and is buffered by U2 which has a closed-loop voltage gain of one but a near zero ohm output impedance.

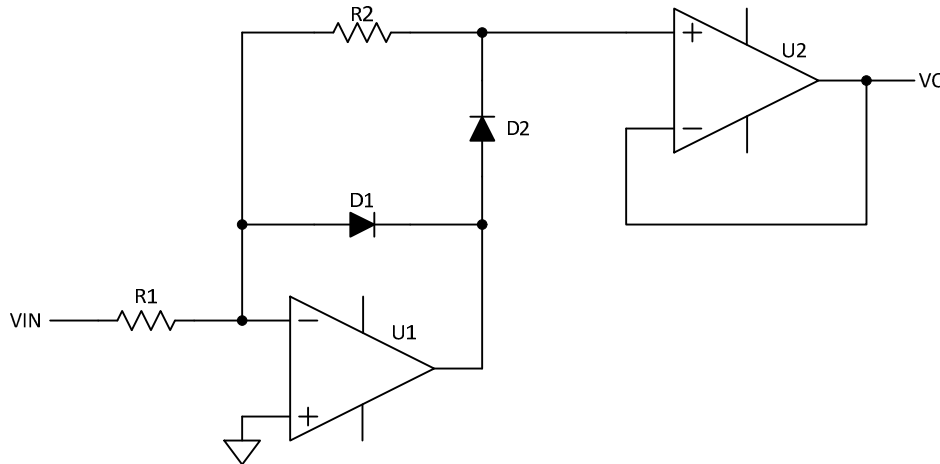


Figure 14: Precision half-wave rectifier

Absolute value circuit

The circuit in Figure 15 is an extension of the precision half-wave rectifier to be a full-wave rectifier better known as an absolute value circuit because of its application in analog computational circuits. All the resistors are the same value, generally something in the 2,000 to 10,000 ohm range although R1 could be a different value depending on desired scaling.

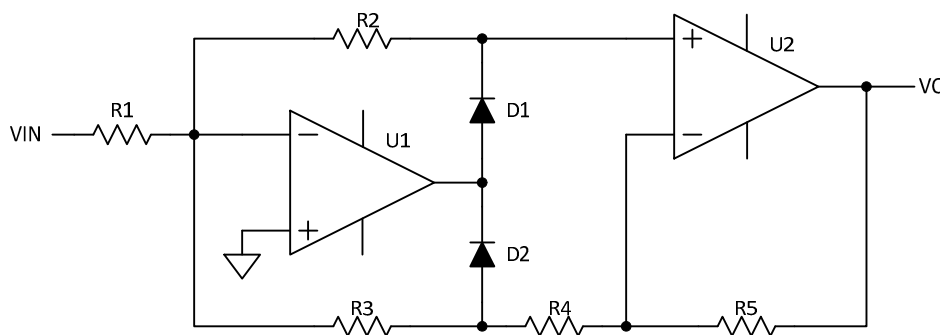


Figure 15: Absolute value circuit

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Logarithmic circuit

The circuit in Figure 16 utilizes the natural exponential characteristic of D1 to produce an output signal, V_O , that is a logarithmic version of V_{IN} . The log function can have any scale factor and offset. A typical circuit might have a scale factor of 1 volt per decade of input voltage and an offset such as shown in the following table. More advanced circuits use a bipolar junction transistor which has more accurate and consistent exponential characteristics than a standard diode.

V_{IN}	V_O
10	5
1	4
0.1	3
0.01	2
0.001	1

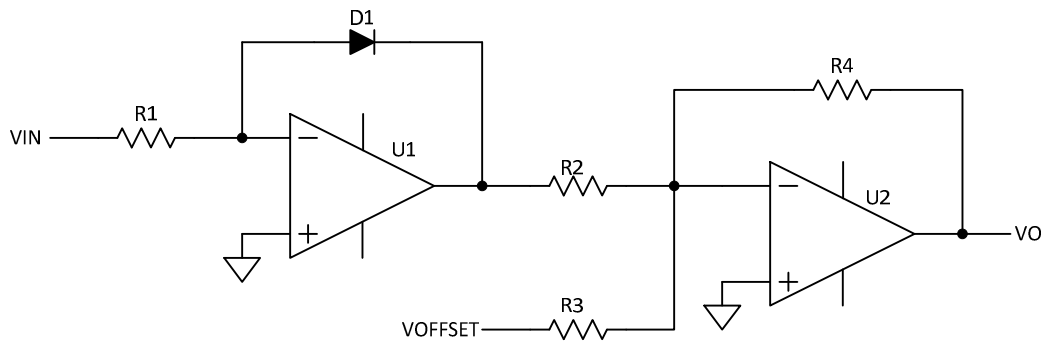


Figure 16: Simple logarithmic circuit

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An advanced op-amp

The circuit in Figure 17 includes some extensions to the basic op-amp circuit that increases the gain and improves its ability to both source and sink output current. The transistor Q numbers and resistor R numbers are kept the same as for the simple circuit in Figure 6 to make it easy to observe the simple equivalent circuit in the more complex circuit.

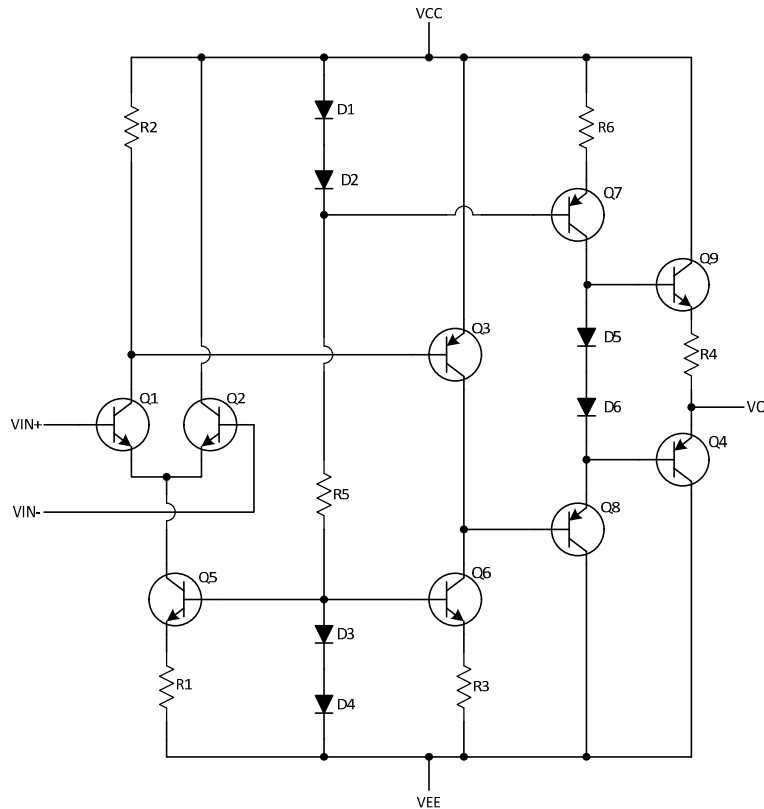


Figure 17: Advanced op-amp

The key improvements in the advanced circuit compared to the simple circuit are:

- Op-amps are generally designed to operate over a wide range of power supply voltages, not just the +15 and -15 volts used in the previous example. Resistors are replaced with current sinks to make the bias conditions independent of power supply voltages. Bias voltages for the current sinks are derived from the forward voltage of a diode. The starting point is the series circuit of D1, D2, R5, D3, and D4. The voltage at the base of Q7 is ~ 1.2 volts below VCC. The voltage at the bases of Q5 and Q6 is ~ 1.2 volts above VEE. Thus the collector current of Q7 is fixed at $\sim 0.6/R6$ and the collector current of Q5 is fixed at $\sim 0.6/R1$ and the collector current of Q6 is fixed at $\sim 0.6/R3$. This enables the circuit to operate from a difference between VCC and VEE of less than 10 volts to over 30 volts. VCC and VEE do not have to be the same magnitude – VCC might be +12 and VEE might be -5 in a particular application – the amplifier circuit does not care.
- By making the current from the emitters of Q1 and Q2 fixed means that operation is not dependent on the actual voltage at the bases of Q1 and Q2 as in the simple circuit.

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- Using a current sink (Q6) for the load on Q3 instead of a finite resistance (R3) enables the voltage gain of Q3 to be much higher.
- The use of a parallel common-collector stage (Q9) to Q4 in place of the original R4 enables the output to both drive and sink substantial current. R4 in this case is a small value (a few tens of ohms) that prevents a bad situation of both Q9 and Q4 conducting at the same time. At any given time only one of the output transistors is conducting. This structure overcomes the issues of determining a fixed emitter resistor in previous single stage circuits. Diodes D5 and D6 fix the voltage between the two transistor bases at ~ 1.2 .
- The use of an additional common-collector buffer (Q8) with a current sink load (Q7) substantially increases the load impedance on Q3 thus enabling very high voltage gain with its current sink load (Q6).

Conclusion

We start with understanding simple single stage amplifiers and then build on that to produce multistage amplifiers and then develop a highly useful generic multistage amplifier known as an op-amp.