

Multistage Amplifier Analysis Example

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Introduction

This note describes how to analyze a direct coupled multistage amplifier built with NPN and PNP transistors as shown in Figure 1. The example circuit explores various issues of how to handle direct coupling. The key is analysis by partition.

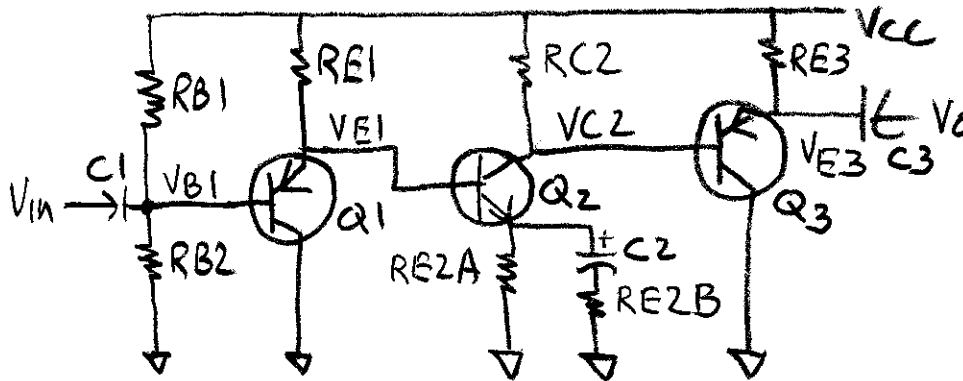


Figure 1: High input/low output impedance amplifier

$V_{CC}=15$ V, $R_{B1} = 360$ K, $R_{B2} = 36$ K, $R_{E1} = 18$ K, $R_{E2A} = 3.6$ K, $R_{E2B} = 47$ Ohms,
 $R_{C2} = 24$ K, $R_{E3} = 1$ K, $C1 = 0.1$ uF, $C2 = 10$ uF, $C3 = 0.1$ uF,
 $Q1 = 2N3906$, $Q2 = 2N3904$, $Q3 = 2N3906$

For analysis we start at the input of the amplifier and work our way to the output. The goals of analysis are to determine the black box characteristics (R_{in} , R_o , A_v) and the various bias voltages in the circuit.

We will take the beta of the transistor to be 150 and V_{BE} to be 0.65 volts.

Bias Analysis of First Stage

The first thing to do is to calculate the bias conditions of Q1. We first compute the open circuit voltage, V_{BB1} , for the base circuit. This is

$$V_{BB1} = 15 * 36 / (360 + 36) = 1.364 \text{ volts.}$$

We then calculate R_{B_Q1} as

$$R_{B_Q1} = 36\text{K} || 360\text{K} = 32.73\text{K}$$

Multistage Amplifier Analysis Example

For the emitter circuit we have a direct coupled second stage whose characteristics we do not yet know. The first stage is a common-collector amplifier and these can be difficult to analyze unless we make a simplifying approximation. For a “well designed” amplifier, the bias loading effects of the next stage are small – often negligibly small. By definition, a “well designed” amplifier has minimal dependence on particular transistor characteristics among other traits. We will assume that this is a “well designed” amplifier (it is). After we have done bias calculations, we can verify this (or not) by using the results to recalculate the bias conditions on the first stage. If the new answer does not change much then our approximation was good.

So, we will ignore the second stage and calculate the emitter current of Q1 as

$$I_{E1} = (1.364 - 15 + 0.65) / (18K + 32.73K/151) = -0.713 \text{ mA}$$

The polarities in this equation may at first not seem right to some students. But note that the 15 volt power supply is the V_{EE} for that stage since that is where the emitter connects to. Because the transistor is PNP we add V_{BE} rather than subtract it. Think of the numerator as the voltage across R_E measured relative to V_{EE} (+15 volts in this case).

We now compute the voltage at the emitter of Q1 or base of Q2 – take your pick. We generally like to measure voltages relative to ground so the voltage at the base of Q2 is

$$V_{B2} = 15 - 0.713 \text{ mA} * 18 \text{ K} = 2.17 \text{ volts}$$

The last thing to do is calculate the voltage at the base of Q1 relative to ground. This voltage will be somewhat higher than the open circuit voltage calculated earlier because the base current is out of the transistor for a PNP rather than in. This voltage is

$$V_{B1} = 2.17 - 0.65 = 1.52 \text{ volts}$$

Bias Analysis of Second Stage

We are finished with bias calculations for the first stage. The next thing to determine is the effective R_B for Q2. This is much smaller than the 18 K emitter resistor for Q1. The correct value is the DC output resistance of the Q1 stage which is the emitter resistor (18 K) in parallel with the base resistance divided by $B+1$ ($32.73 \text{ K} / 151 = 217 \text{ ohms}$). Thus the effective R_B for Q2 is

$$R_{B_Q2} = 18,000 \parallel 217 = 214 \text{ ohms}$$

Note that this value is negligibly small compared to R_{E2} (3.6 K) and is a characteristic of a well designed amplifier. Thus, the effect of the Q2 base current on the bias condition for the first stage discussed earlier is negligible. We had to assume that at first. Now it is proved. If this were not the case then our bias calculations for stage 1 would not be right and we would have to resort to more math and probably iteration to obtain the correct

Multistage Amplifier Analysis Example

results. The R_{B_Q2} term is included in the following calculation only so as not to confuse the student – note that $214 / 151$ is negligibly small compared to the 3.6 K emitter resistor.

$$I_{E2} = (2.17 - 0.65) / (3.6 \text{ K} + 214 / 151) = 422 \text{ uA}$$

The emitter voltage of Q2 is the same as the base voltage of Q1 or 1.52 volts – practically independent of temperature! This is achieved by the right combination of PNP and NPN transistors in a circuit to realize a net result better than either alone.

Now we calculate the bias condition at the collector of Q2. The first thing to do is to calculate the collector current by multiplying the emitter current by $B/(B+1)$. This results in an I_{C2} of 419 uA.

Bias Analysis of Third Stage

At this point we can calculate an open circuit (i.e. base of Q3 not connected) voltage for the collector of Q2. The actual voltage can not be determined until we know the bias conditions for Q3. The open circuit (or Thevenin) voltage of V_{C2} is the same as the V_{BB} for Q3. R_B for Q3 is simply the collector resistor of Q2 since the collector of Q2 appears as a current source or infinite (well, at least very large) resistance.

$$V_{BB_Q3} = 15 - 419 \text{ uA} * 24 \text{ K} = 4.94 \text{ volts}$$

We now calculate the emitter current for Q3 as

$$I_{E3} = (4.94 - 15 + 0.65) / (1000 + 24\text{K} / 151) = -8.12 \text{ mA}$$

The emitter voltage of Q3 with respect to ground is

$$V_{E3} = 15 - 8.12 \text{ mA} * 1 \text{ K} = 6.88 \text{ volts}$$

The voltage at the base of Q3 will be higher than the open circuit voltage, V_{BB3} calculated earlier since this is a PNP transistor and is

$$V_{B3} = 6.88 - 0.65 = 6.23 \text{ volts}$$

AC Analysis

This completes the bias analysis. We are now ready for AC analysis. First, we calculate the dynamic resistance of each of the transistors

$$r_{e1} = 0.026 / 0.713 \text{ mA} = 36.5 \text{ ohms}$$

$$r_{e2} = 0.026 / 0.422 \text{ mA} = 61.6 \text{ ohms}$$

$$r_{e3} = 0.026 / 8.12 \text{ mA} = 3.2 \text{ ohms}$$

Multistage Amplifier Analysis Example

Calculation of input resistance of the amplifier

Since the first stage is common-collector we need to know the impedance in the emitter circuit first which will be 18 K in parallel with the input impedance of the second stage. The input impedance of the second stage is found the usual way as

$$r_{bt2} = 151 * (61.6 + 3600 \parallel 47) = 16.3 \text{ K}$$

The input impedance of the first stage is found the usual way as

$$r_{bt1} = 151 * (36.5 + 18 \text{ K} \parallel 16.3 \text{ K}) = 1.3 \text{ M}$$

The net input resistance of the amplifier is then the RB of the first stage in parallel with r_{bt1} which is

$$R_{in} = 32.7 \text{ K} \parallel 1.3 \text{ M} = 31.9 \text{ K}$$

Calculation of output impedance of the amplifier

The output resistance of the amplifier is simply the output resistance of the common-collector output stage which is calculated as

$$R_o = 1000 \parallel (3.2 + 24 \text{ K} / 151) = 139.5 \text{ ohms}$$

Calculation of unloaded voltage gain, A_v , of the amplifier

The voltage gain of the first stage is

$$A_{v1} = 18\text{K} / (36.5 + 18 \text{ K}) = 0.998$$

The output resistance of the first stage is at most (taking the source resistance, which we do not know, to be very large compared to the RB of the first stage) given by the following

$$R_{o1} = 18\text{K} \parallel (36.5 + 32.73 \text{ K} / 151) = 249.7 \text{ ohms}$$

The input resistance, r_{bt2} , to the second stage has already been calculated as 16.3 K.

The voltage division factor between first and second stages is

$$V_{d12} = 16.3 \text{ K} / (249.7 + 16.3 \text{ K}) = 0.985$$

Multistage Amplifier Analysis Example

The voltage gain of the second stage is

$$A_{v2} = (150 / 151) * 24 \text{ K} / (61.6 + 3600 \parallel 47) = 220.8$$

The output resistance of the second stage is 24 K.

The input resistance of the third stage is

$$R_{in3} = 151 * (3.2 + 1000) = 151.5 \text{ K}$$

The voltage division factor between the second and third stages is

$$V_{d23} = 151.5 \text{ K} / (24 \text{ K} + 151.5 \text{ K}) = 0.863$$

The voltage gain of the third stage is

$$A_{v3} = 1000 / (3.2 + 1000) = 0.997$$

The total voltage gain of the amplifier is

$$A_v = 0.998 * 0.985 * 220.8 * 0.863 * 0.997 = 186.7$$

Summary Results

$$R_{in} = 31.9 \text{ K ohms}$$

$$R_o = 139.5 \text{ ohms}$$

$$A_v = 186.7$$

Further exercise for the student

The student should create an equivalent circuit using NPN-PNP-NPN stages and swap the location of ground and VCC (hint: redraw the circuit to resemble this one). Then analyze that circuit using the same process as described here. The method and the results will be identical except for obvious polarity differences. Some voltages will be different since the reference point has moved with the VCC and ground swap but that should make complete sense. For example, V_{B2} will become $15 - 2.17 = 12.83$ volts.