Analysis and Design of a Simple Operational Amplifier

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Introduction

The purpose of this article is to introduce the student to the internal circuits of an operational amplifier by studying the analysis and design of a very simple circuit. Techniques of analysis and design are demonstrated in detail.

In its simplest form, an operational amplifier consists of three amplifier stages. The first stage is the differential input amplifier which amplifies the difference between the two input signals but rejects the commonality or common-mode portion of the input signals. The second stage is designed for high voltage gain. The third stage is designed for low output impedance.

Analysis

The circuit that will be studied is shown in Figure 1. This circuit is about as simple as an operational amplifier can be. Transistors, Q1 and Q2, form the input differential amplifier with Q3 providing constant current bias. Transistors, Q4 and Q5, are the second stage and provide high voltage gain. Transistor, Q6, is the third stage and is a common collector amplifier that provides low output impedance. Transistor, Q7, provides constant current biasing for Q6.

Never attempt to analyze a circuit such as this as a whole as that is too complicated and frustrating. Analysis will be performed by partitioning the circuit into its fundamental parts. Using this method reduces a complicated circuit to a series of simple calculations. The student must carefully work through these calculations and learn as much as possible. The original calculations were done with more resolution than shown on this paper and may not exactly match repeat calculations because of round-off.

The first question is where to begin. The short answer is to trace through the circuit and locate the most fundamental section. This is an acquired skill that can only be perfected through experience – i.e. choosing the wrong starting point and then having to start the analysis over at a new point (perhaps not the right place again). To keep the analysis simple we will use 150 for the beta of all transistors and assume that the VBE of all transistors is 0.65 volts. There are some small errors inherent in this but our goal is understanding of the circuit instead of extreme accuracy.

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Analysis of the bias voltage divider

For this circuit the most fundamental starting point is the voltage divider comprised of RB1 and RB2. The unloaded output voltage is 30V * 2,200 / (43,000 + 2,200) = 1.46 volts. This voltage provides bias for transistors, Q3 and Q7. The source resistance of this voltage divider is 43,000 || 2,200 = 2093 ohms.

Analysis of the current sinks

We will calculate the total emitter current of both transistors by combining the circuits into a single transistor stage using the parallel equivalent of emitter resistors RE1 and RE3. Thus, the emitter resistance for this calculation is 2,700 || 150 = 142.11 ohms. The total emitter current is found by:

IE(total) = (1.46 – 0.65) / (142.11 + 2,093/151) = 5.195 mA.

The individual emitter currents are determined by using current division.

IE3 = 5.195 mA * 142.11 / 2700 = 0.273 mA

IE7 = 5.195 mA * 142.11 / 150 = 4.921 mA

Because the bias of transistors, Q3 and Q7, is fixed, the collector currents will be fixed or constant. The constant collector currents are:

IC3 = (150 / 151) * 0.273 mA = 0.272 mA

IC7 = (150 / 151) * 4.921 mA = 4.889 mA

Stage 1 analysis

We will now analyze the differential input stage. For simplicity we will assume that transistors, Q1 and Q2, conduct equal currents. This is the design target and is roughly true in reality. Thus, the emitter current of each transistor is half of IC3 or 0.136 mA. Each base current will be 0.136 mA / 151 = 905 nA – this is the input bias current of the amplifier. Each collector current will be (150/151) * 0.136 mA = 0.135 mA. The unloaded voltage drop across each collector load resistor is 0.135 mA * 11,000 ohms = 1.48 volts.

The dynamic emitter resistance of each transistor is 0.026 / 0.136 mA = 191.5 ohms. The unloaded differential voltage gain is (150/151) * 11,000 / 191.5 = 57. The differential input resistance is 151 * 2 * 191.5 = 57,823 ohms. The differential output resistance is 2 * 11,000 = 22,000 ohms.

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Stage 2 analysis

Transistors, Q4 and Q5, provide high voltage gain. These are PNP transistors and for simplicity, the analysis will be turned upside down and the 1.48 volts dropped across each collector resistor, RC1, of the first stage will be the VBB for each transistor and the 11,000 Ohm collector resistor will be the RB driving each transistor. Calculation of the emitter current of each transistor is similar to that of a single transistor amplifier but is modified to accommodate two transistors with a common emitter resistor. The total emitter current of both transistors is:

IE(total) = (1.48 – 0.65) / (360 + 11,000/(2 * 151)) = 2.103 mA

Thus, the emitter current of each transistor is 1.052 mA and the collector current of each transistor is (150/151) * 1.052 mA = 1.045 mA.

The unloaded voltage across RC2 is 1.045 mA * 15,000 = 15.67 volts.

The dynamic emitter resistance of each transistor is 0.026 / 1.052 mA = 24.7 ohms. The unloaded voltage gain at the collector of Q5 is (150/151) * 15,000 / (2 * 24.7) = 301. The differential input resistance of the second stage is 151 * 2 * 24.7 = 7,466 ohms.

Stage 3 analysis

Transistor, Q6, has a constant current emitter bias of 4.889 mA as previously calculated. Thus, the base current of Q6 is 4.889 mA / 151 = 0.032 mA. Thus, the emitter voltage of Q6 is:

VE = 15.67 V – (0.032 mA * 15,000 ohms) – 0.65 = 14.54 volts

The voltage gain of the third stage is 1.0 because the effective emitter resistance is infinity because of the constant current biasing. The dynamic emitter resistance is 0.026 / 4.889 mA = 5.32 ohms. The output resistance of the amplifier is 15,000 ohms / 151 + 5.32 ohms = 105 ohms. The input resistance of the third stage is taken to be infinity because of the constant current emitter biasing.

Overall voltage gain

The overall voltage gain of this amplifier is the product of the gain of the first stage, the voltage division to the second stage, and the gain of the second stage. As previously discussed, the third stage has a voltage gain of 1.0 and essentially infinite input resistance and so there will be no input voltage division. The total differential gain of the amplifier is Av = 57 * [7,466 / (22,000 + 7466)] * 301 = 4,358.

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Summary

Ignoring finite bandwidth, the entire amplifier can be represented by a black box that has a differential input resistance of 57,823 ohms, an output resistance of 105 ohms, and a voltage gain of 4,358.

Design

The design of this amplifier will proceed in the reverse order of analysis.

The specifications we will implement will be to perform a bias design for the given operational amplifier circuit to operate on a 30 volt supply. The output stage should have an output resistance of around 100 ohms and be able to source or sink up to 5 mA to a load. The gain should be as high as practical but is not specified – we do not have much control over it in this circuit – we get what we get. As long as the gain is high then it really does not matter much what the exact gain is so we do not worry about it. We would also like the differential input resistance to be as high as practical but again we do not have much control in this circuit – we get what we get. The good news is that as long as we follow a good procedure then these uncertainties will not generally be an issue. With a more complex circuit we could address these uncertainties but our goal here is to understand the basic design criteria for a simple amplifier. Other desirable traits would be to have low input offset voltage and low input bias current but we have little if any control over these with this simple circuit.

Before delving into the design procedure, it is useful to discuss what we are trying to do and why. Design is much easier if we understand what we are doing. It should be understood that our design specifications are targets rather than absolute requirements.

For example, the 5 mA peak output current and 100 Ohm output resistance are based on the amplifier driving plus or minus 10 volts into a 2,000 Ohm load – a common value that most standard operational amplifiers can do. It is good practice for the output resistance of the amplifier to be around one-tenth or less of the lowest resistance load the amplifier will drive. In this case the target specification is five percent. While it is possible to refine the design to achieve exactly 100 ohms, that is not necessary. It will make no difference if the output resistance is smaller or higher by some reasonable amount. We will only worry about precision where it really does matter. The 5 mA peak output current specification is a typical and reasonable value for common op-amps. Again, we will not strive to achieve that precise amount. Rather, we understand that specification to imply not much less than about 5 mA so we will actually design to a slightly larger value. The key to successful design is to understand what specifications are meant to be achieved with high precision and what specifications are general targets. It is folly to waste time trying to achieve high precision for a general target.

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Stage 3 design

We note that stage 3 is a common-collector amplifier that utilizes a constant current sink for setting the quiescent emitter current. Thus, the peak current that the amplifier can sink from a load is the magnitude of the current sink. The peak current that the amplifier can source to the load will generally be much higher but we are interested only in what can be done symmetrically, so the magnitude of the current sink should be set to at least 5 mA. We will add a margin of ten percent so the current source will be designed using a target of 5.5 mA. This means that the dynamic emitter resistance of Q6 will be 0.026 V / 5.5 mA = 4.7 ohms.

The output resistance of the amplifier is simply the value of RC2 divided by B+1 and added to the dynamic emitter resistance. The resistance of the current sink is taken to be infinity (or at least very large). The only control over output resistance we have then is the value of RC2. We can calculate RC2 as (100 – 4.7) * 151 = 14,386 ohms. We will round this value to 15,000 ohms.

In the interest of balance, we generally design for the quiescent output voltage to be either zero volts (if we are using symmetrical positive and negative power supply voltages) or to be half way between the two power supply voltages otherwise. This is a sensible value to choose and is the only one I know of that can be justified without sounding stupid. However, it is not a critical choice and so only a token effort should be made in achieving this. The significance of this is that we now have a basis for choosing the quiescent collector current of Q5 (with balance the same current will also be through Q4). So, in our circuit, the quiescent voltage at the emitter of Q6 should be 15 volts. Thus, the voltage at the base of Q6 should be 15.65 volts. The base current for Q6 is 5.5 mA / 151 = 34.6 uA. The current through RC2 is 15.65 / 15,000 = 1.043 mA. Thus, the collector current for Q5 should be the sum or 1.08 mA.

There is one final thing to discuss about the choice for the quiescent output voltage. This particular design was based on a total power supply voltage of 30 volts. In reality it is generally desirable for the amplifier to operate satisfactorily over a range of power supply voltages. In this situation, a good choice is to use the average of the range of power supply voltages. Remember also that this note is based on the lower supply being zero volts. The upper supply was 30 volts for a total power supply voltage of 30 volts. A more typical example might have the upper supply at 15 volts and the lower supply at -15 volts for a total power supply voltage of 30 volts. The analysis is made easier by adding the appropriate amount to both power supply voltages such that the lower supply becomes zero. Then there is only one power supply voltage to be concerned with. This has no effect on the actual operation of the amplifier since all the voltages are relative across the part anyway.

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Stage 2 design

The design of stage 3 dictates that the quiescent collector current of Q5 and Q4 be 1.08 mA. Thus, the current through RE2 is 2 * (151/150) * 1.08 mA = 2.17 mA. We must first determine a reasonable VBB for Q4 and Q5 and then calculate the required value of RE2 to achieve the specified collector currents. We will use our past experience with transistor design which lets us choose a VBB of 1.5 volts with the comfort that the design will be reasonably temperature stable. We were not given a temperature specification to design to so that must not have been very important. All we can do here is make a reasonable choice.

The calculation of RE2 is similar to that of a single transistor amplifier. We will make the appropriate modification for the fact that two transistors are involved. Before proceeding with the calculation of RE2, we must know the resistance of RC1 which becomes the RB for this stage. We can not know that value until we know RE2. We escape this dilemma by using ratios. We know from our previous study of transistor bias design that an RB/RE ratio of 13 was fairly conservative. For convenience, we will round this to a nice value of 15 (we could justify choosing even higher but that would digress from our present goal of understanding). Since we have two transistors, each contributing half of the total, then the RB for each transistor could be 30 times the RE2 value we calculate. Using this and the fact that RE2 conducts twice the current of a single transistor, we can calculate RE2 as:

RE2 = (1.50 – 0.65) / (2 * 0.001087 * (1 + 30 / (2 * 151))) = 355.7 ohms.

We will round this to the standard value of 360 ohms. We then multiply this by 30 to obtain 10,800 ohms for RC1. We will round this value to the standard value of 11,000 ohms.

Stage 1 design

To achieve the 1.5 volt VBB chosen for stage 2 then the collector current of Q1 and Q2 must be 1.5 / 11,000 = 136 uA. The emitter current will then be 137 uA. The collector current of the current sink, Q3, then must be twice this value or 275 uA. The base current for each transistor is found by dividing the collector current by 150 and is 916 nA. This is the input bias current for this operational amplifier.

Design of the current sinks

The emitter current for Q3 will be 276 uA. The emitter current of Q7 will be (151/150) * 5.5 mA = 5.537 mA. The total emitter current for both transistors is 5.813 mA. For reduced parts count, both transistors are driven by the same voltage divider. This makes the bias design slightly more complicated than that for a single transistor. With a little thought it should be realized that a design based on the sum of the emitter currents can be

done and then current division can be used to determine the specific RE1 and RE3 values. We will again use a VBB of 1.5 volts and an RB/RE ratio of 15 for the same reasons discussed earlier. We can now calculate the resistance of RE1||RE3 by using our single stage transistor design notes

RE1||RE3 = (1.5 – 0.65) / (0.005813 * (1 + 15 / 151))) = 133 ohms

Using current division we can calculate RE1 as 133 * (5.813 mA / 0.276 mA) = 2,801 ohms. We will round this value to 2,700 ohms. We can calculate RE3 as 133 * (5.813 mA / 5.537 mA) = 140 ohms. We will round this value to 150 ohms.

Design of the bias voltage divider

The actual parallel resistance of RE1 and RE3 is 2700 || 150 = 142 ohms. The required source resistance of the voltage divider is 15 times this or 2,132 ohms. The ratio, RB1/RB2 is found by 30 / 1.5 – 1 = 19.0. RB1 is calculated as 2,132 * (30 / 1.5) = 42,600 ohms. We round this to the standard value of 43,000 ohms. RB2 is calculated as 43,000 / 19.0 = 2,263 ohms. We round this to the standard value of 2,200 ohms.

Verifying the design

The last step in any design is to perform an analysis to verify that the results are in agreement with the specifications. This analysis has already been presented earlier in this paper. Note from the analysis that the peak output current is a bit less than the target value of 5 mA. This is the result of various round-off errors. If it were really important for the output peak current to be 5 mA or larger then we could either obviously reduce RE3 to 130 Ohms or perhaps (less obviously) increase RB2 to 2,400 Ohms. There are other small shifts in component values that would also achieve this.

The best way to make a determination of what to tweak is to write a detailed spreadsheet like the one illustrated at the end of this paper. The problem with tweaking is that some side effects might be undesirable. With a complete spreadsheet then all effects of any change can immediately be seen. This particular spreadsheet was used to design this amplifier and then verify the results through analysis. Although all the calculations are simple, the probability of a mistake approaches 100% when they are done by hand. Once all the bugs are out of a spreadsheet then many scenarios can be tested very easily. A copy of the spreadsheet is at the end of this article.

Improvements in the design

Here are some of the things that an integrated circuit design would incorporate to provide improved performance over this design.

- Q1 and Q2 would be specially designed to have high beta for lower input bias current. They would also be matched for low input offset voltage.
- Bias nulling circuits would be incorporated on the two inputs to further reduce the input bias current.
- Protective circuits would be at the input to limit excessive differential voltage.
- Laser trimming would be used to reduce the input offset voltage to as small as practical.
- More advanced bias circuits would be used to better stabilize the bias over a range of power supply voltages
- An additional voltage gain stage might be used to achieve much higher voltage gain.
- The output amplifier would consist of two common-collector amplifiers biased to class AB operation for higher output current drive without using a current sink.
- Current limiters would be used on the output to prevent damage to Q6 in case of an overload.

Testing the amplifier

The amplifier circuit in Figure 1 was built and tested. Any circuit such as this will need some kind of frequency compensation to remain stable at low closed loop gains. Frequency compensation is not a part of this paper and so details will not be discussed. This particular amplifier was found to have a small 30 MHz oscillation when the closed loop gain was 1. For the DC tests in Figure 2 frequency compensation was added to prevent artificial offsets caused by nonlinearities in the oscillation. For the AC tests the amplitude of this oscillation was small enough that it was deemed non problematic for these simple tests and the frequency compensation was removed. There was no oscillation when the closed loop gain was ten. Here is a summary of the results.

The measured value of IE3 was 0.312 mA. This compares with the calculated value of 0.273 mA. The measured value of IE4 + IE5 was 2.56 mA meaning that each emitter current is about 1.28 mA. This compares to the calculated value of 1.052 mA. The measured value of IE7 was 5.29 mA. This compares with the calculated value of 4.921 mA.

The circuit in Figure 2 was used to measure the bias currents and input offset voltage. The input bias current IB+ was measured to be 1.025 uA. The input bias current, IB-, was measured to be 0.944 uA. Thus, the spec input bias current which is the average of the individual bias currents is 985 nA. This compares to the calculated value of 905 nA. The input offset current is the difference between the individual bias currents and is 81 nA. The input offset voltage was measured to be 1.8 mV which is remarkably low for a

discrete circuit without special matching of the input transistors. This must have been a case of pure luck as an offset ten times this value would have been reasonable.

The circuit in Figure 3 was used to measure the open loop gain and frequency response of the amplifier. The purpose of the auxiliary op-amp is to be a high impedance buffer for the integrated charge on the capacitor. Otherwise, the input impedance of the op-amp under test causes an error. The feedback network is designed to stabilize the output DC voltage to be near zero volts while providing no AC feedback thus permitting the open loop gain and frequency response to be measured. When the circuit is first turned on the feedback resistor is briefly shunted with a 1 K resistor to allow the capacitor to quickly charge to the required value – otherwise it could take many tens of minutes before testing could be done. Without the DC stabilization circuit the output of the op-amp will be at either the positive or negative maximum. The open loop gain was measured to be 4,800 which compares to the calculated value of 4,358. The actual gain would be expected to be somewhat higher than the original calculation since the actual emitter currents were somewhat higher than calculated. The -3 dB frequency was measured to be 43 kHz. Thus, the gain-bandwidth product of this amplifier is 206 MHz. The gain at 100 kHz was 2,050 and the gain at 1 MHz was 200. Note that the gain drops off by a factor of ten for a factor of ten increase in frequency as would be expected for a first order roll-off. This circuit was not designed for any particular bandwidth. It was expected that the gain bandwidth product would be in the single or perhaps double digit Megahertz range. It was a surprise that it turned out to be over 200 MHz. A contributing factor is that the currents for the first and second stages are higher than might be found in a low bandwidth monolithic op-amp. Higher currents and the resulting lower impedances contribute to higher bandwidth.

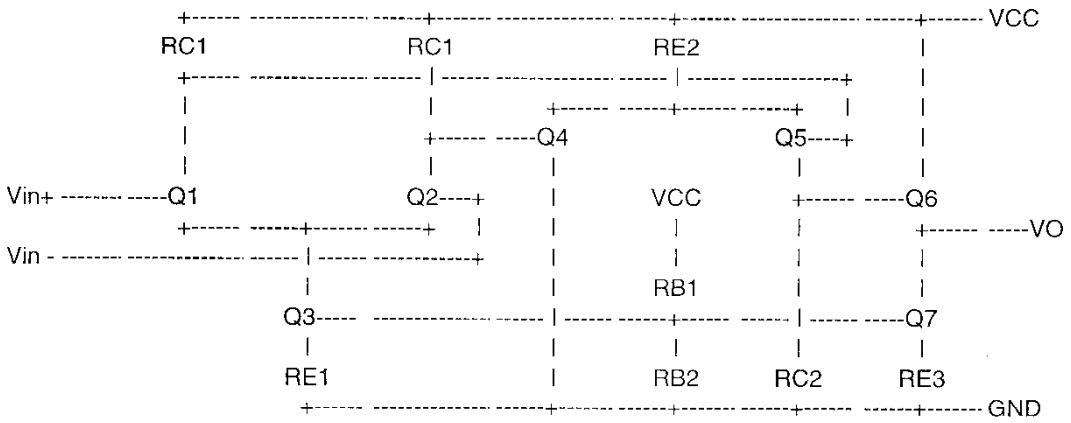
A 1 K load resistor was added to the circuit of Figure 3 and the output voltage dropped to 95 percent of the unloaded value at a frequency of 1 kHz. Using voltage divider math this means that the output resistance of the amplifier is 53 Ohms which is about one half the expected value. This is better than designed but there is not a good explanation. The actual beta of the transistors was around 220 and this would have lowered the output resistance somewhat from the design value using a beta of 150 but not by a factor of 2 – but this is only a simple analysis.

Conclusion

Although it is very unlikely that anyone would need to design a discrete component operational amplifier such as this in real life it is useful to explore the issues to better understand real operational amplifiers using integrated circuit technology. The discrete version will have significant error terms in comparison to the integrated circuit version. Because of its simplicity, low gain, and easy to measure errors, a simple operational amplifier makes for ideal study. Lessons learned from this exercise can then be applied to real operational amplifiers for the best possible results.

Analysis and Design of a Simple Operational Amplifier

Spreadsheet to design and analyze simple operational amplifiers
opamp design.xls rev. 0 written by Kenneth A. Kuhn



Design:

Specify system constants:

150	Beta (nominal) of all transistors
0.65	Volts, VBE nominal
30	Volts, VCC
15	(RB/RE) for design

Beta calculations:

151	B + 1
0.993	B / (B + 1)

Stage 3 design:

0.005	A, peak output current,specified
1.10	(IE6 / peak output current), typically 1.1
0.005500	Amperes, IE, Q6
0.005537	Amperes, IE, Q7
100	Ohms, Ro, specified
4.73	Ohms, re6, nominal
14386	Ohms, RC2 nominal
15000	Ohms, RC2 actual
36.4E-6	IB, Q6
0.001043	Amperes, I,RC2 for Vo = VCC / 2

Stage 2 design:

0.001080	Amperes, IC, Q4, Q5
7.2E-6	Amperes, IB, Q4, Q5
0.001087	Amperes, IE, Q4, Q5
1.50	Volts, specified VBB for Q4, Q5
355.669	Ohms, RE2 nominal
360	Ohms, RE2 actual

Stage 1 design:

10800	Ohms, RC1, nominal
11000	Ohms, RC1, actual
0.000136	Amperes, IC, Q1, Q2
0.000137	Amperes, IE, Q1, Q2
909.1E-9	Amperes, IB, Q1, Q2 (input bias current)

Analysis: **Design**

Enter actual values: **Values:**

43000.00	Ohms, RB1	43000.00
2200.00	Ohms, RB2	2200.00
2700.00	Ohms, RE1	2700.00
11000.00	Ohms, RC1	11000.00
360.00	Ohms, RE2	360.00
15000.00	Ohms, RC2	15000.00
150.00	Ohms, RE3	150.00
150	Beta	150
0.65	Volts, VBE nominal	0.65
30	Volts, VCC	30

Summary results from below:

4358	Av
57823	Ohms, Rin
105	Ohms, Ro
905.3E-9	Amperes, IB
14.54	Volts, Vo
0.004889	Amperes, peak output current
0.007893	Amperes, power supply

Beta Calculations:

151	B+1
0.993	B/(B+1)

Main bias calculations:

1.46	Volts, VBB, Q3, Q7
2092.92	Ohms, RB
142.11	Ohms, RE1||RE3
0.005195	Amperes, IE, Q3+Q7
0.000273	Amperes, IE, Q3
0.000272	Amperes, IC, Q3
0.004921	Amperes, IE, Q7

Stage 1 calculations:

905.3E-9	Amperes, IB, Q1, Q2

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Main bias design:

0.000275 Amperes, IC, Q3
0.000276 Amperes, IE, Q3
1.50 Volts, specified VBB for Q3, Q7
0.005813 Amperes, IE, Q3+Q7
133 Ohms, RE1||RE3, nominal
1995 Ohms, RB1||RB2, nominal
2798 Ohms, RE1, nominal
2700 Ohms, RE1 actual
140 Ohms, RE3 nominal
150 Ohms, RE3 actual

Design bias network:

19.00 (RB1/RB2)
142.1053 Ohms, RE1||RE3, actual
2131.579 Ohms, RB||RB2, target
42632 Ohms, RB1 nominal
43000 Ohms, RB1 actual
2263 Ohms, RB2 nominal
2200 Ohms, RB2 actual

0.000135 Amperes IC, Q1, Q2
0.000136 Amperes, IE, Q1, Q2

Stage 2 calculations:

1.48 Volts, VBB, Q4, Q5
0.002103 Amperes, IE, Q4+Q5
0.001052 Amperes, IE, Q4, Q5
0.001045 Amperes, IC, Q4, Q5

Stage 3 calculations:

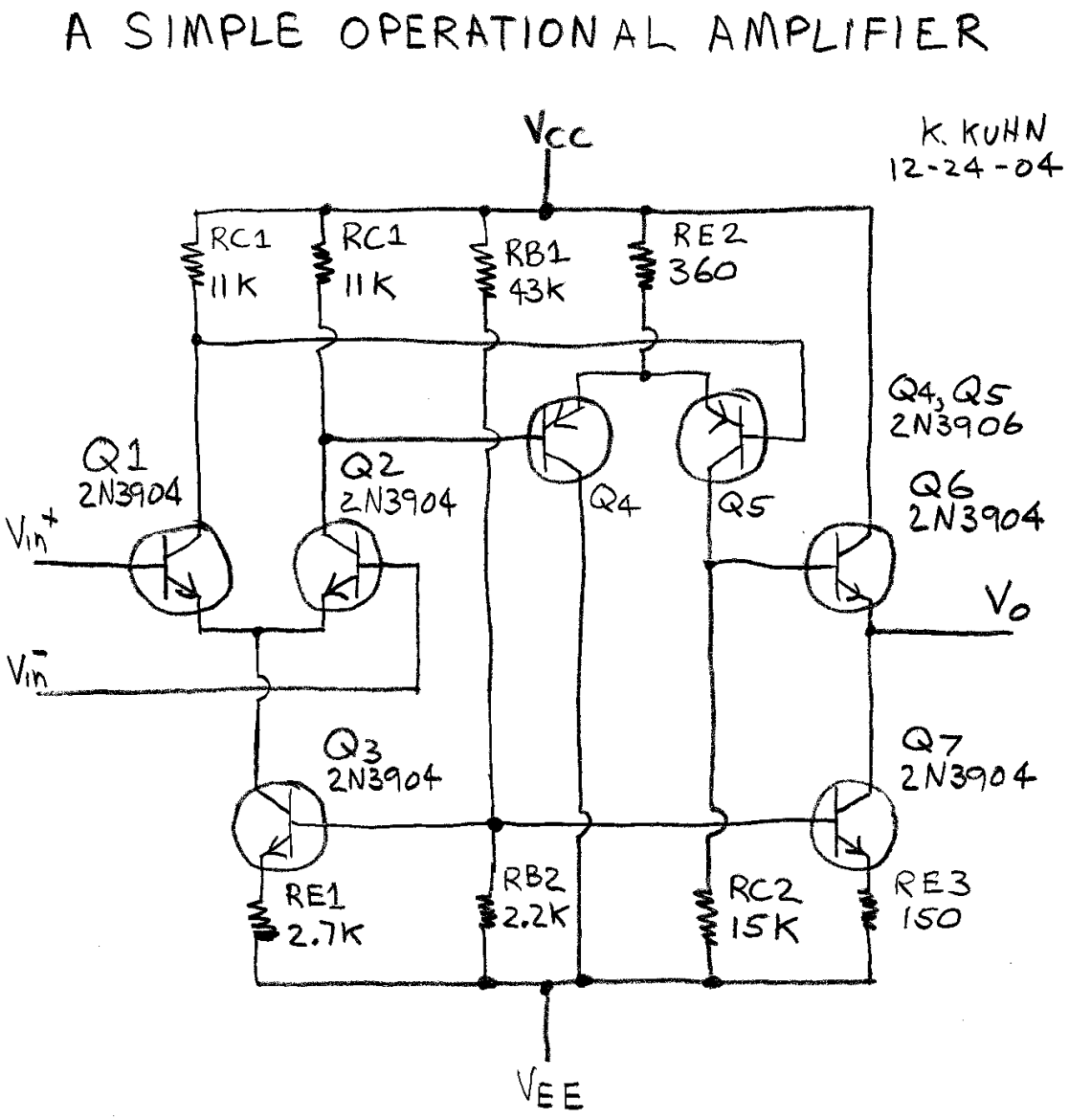
15.67 Volts, VBB, Q6
0.004889 Amperes, IE, Q6
0.000032 Amperes, IB, Q6
14.54 VE, Q6 (V0)

AC calculations:

191.47 Ohms, re, Q1,Q2
24.72 Ohms, re, Q4,Q5
5.32 Ohms, re, Q6
57 Gain, input stage
7466 Ohms, Rin, stage 2
0.253 Voltage division
301 Gain, stage 2
1 Gain, stage 3
4358 total gain
57823 Ohms, Rin
105 Ohms, Ro

Power Supply Calculations:

0.000270 Amperes, IC, Q1+Q2
0.002103 Amperes, RE2
0.004856 Amperes, IC, Q6
0.000664 Amperes, voltage divider
0.007893 Total current



Q_1, Q_2 DIFFERENTIAL INPUT AMPLIFIER

Q_3 CONSTANT CURRENT SINK

Q_4, Q_5 HIGH VOLTAGE GAIN AMPLIFIER

Q_6 LOW IMPEDANCE OUTPUT AMPLIFIER

Q_7 CONSTANT CURRENT SINK

FIGURE 1

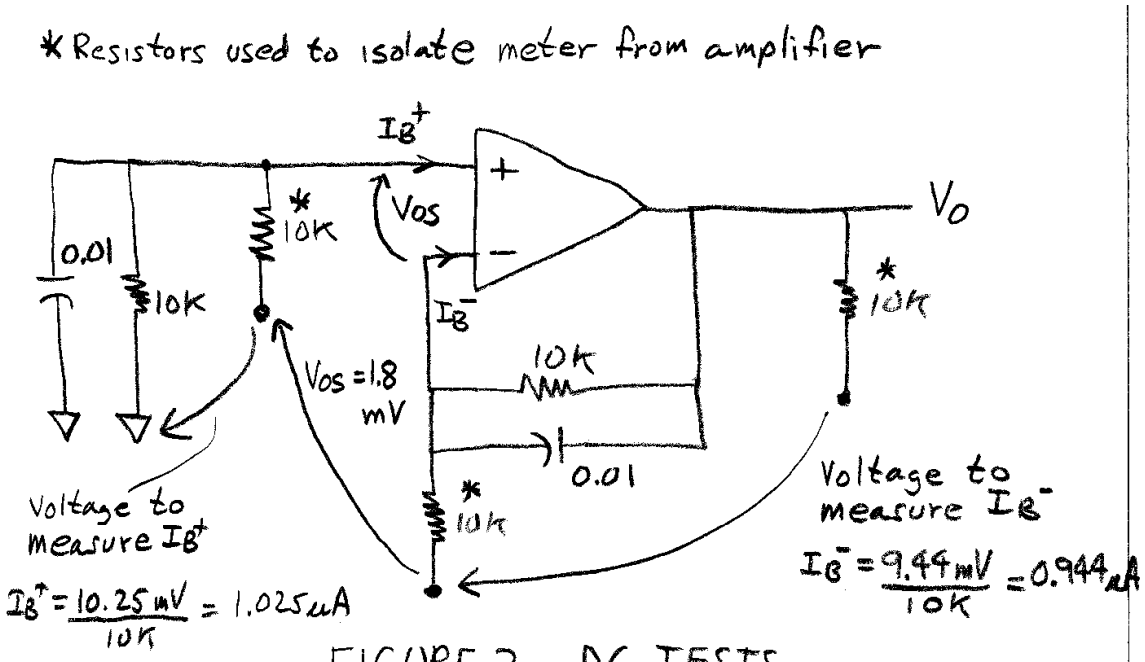


FIGURE 2 - DC TESTS

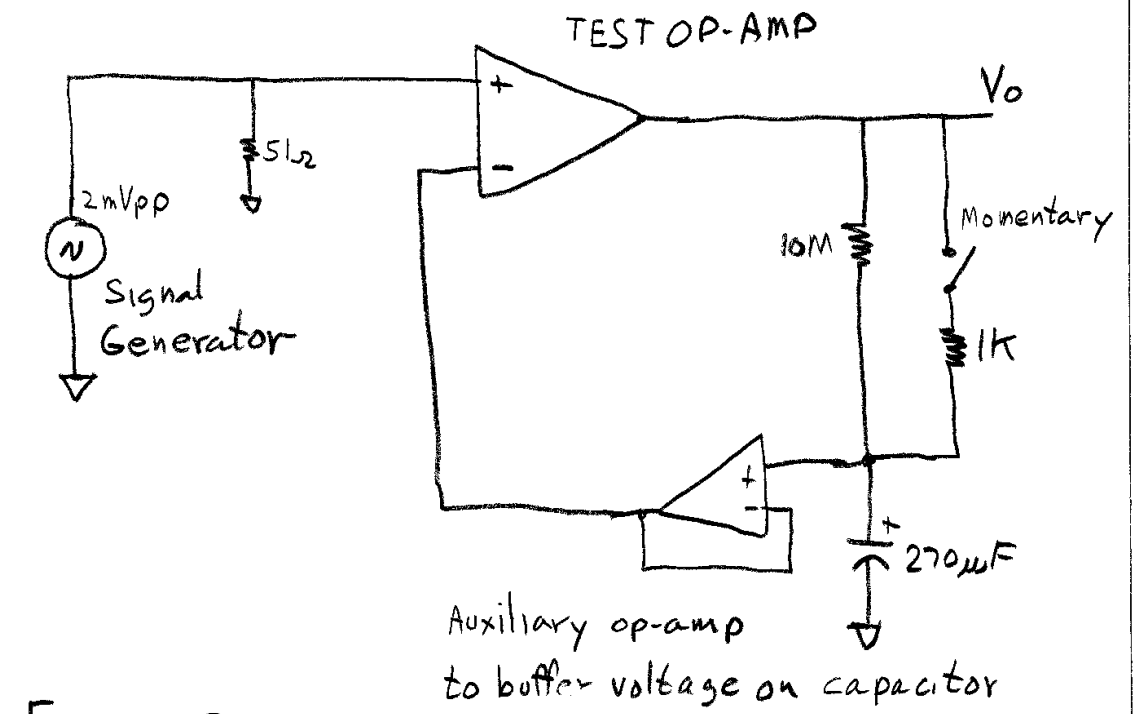


Figure 3 - AC TESTS