Series Voltage Regulators

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April 4, 2009, rev. April 14, 2013

Introduction

The most common form of analog voltage regulation is known as series because the control element (a transistor) is in series with the unregulated voltage source and the load. A high gain proportional control system is used to drive the control element so that the error between the voltage feedback and reference voltage is minimized. Thus, the voltage across the load is very constant – often with only a few millivolts of deviation from no-load to full-load.

Operation

Figure 1 illustrates the simplest possible series regulator. The circuit is simply an emitter follower (i.e. common-collector) amplifier with a fixed low-impedance DC voltage on the base. Thus, the output voltage at the emitter will be the base voltage minus an approximate 0.65 volt base-emitter forward diode drop. This circuit has been often used in a variety of equipment because of its simplicity. It is not capable of holding the output voltage to the exactness of a closed loop controller but its performance is sufficiently good for many applications.

The Zener shunt voltage reference is designed the usual way with the transistor base current being the load. The beta of the transistor will generally be in the 50 to 100+ range so a 1 ampere load current only becomes 10 to 20 mA of base current – well within the range of a simple Zener regulator. The power dissipation of the transistor is the voltage across it multiplied by the current through it. The power dissipation can become significant and proper thermal design including an appropriate heat sink is usually required or else the transistor will quickly overheat and fail.

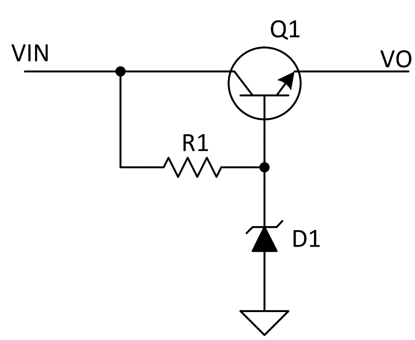

Figure 1: Simplest possible series regulator (open-loop)

A simple closed-loop series regulator is shown in Figure 2. The unregulated input voltage is V_{IN} which may vary up and down several volts from nominal. There is a voltage reference formed by the shunt regulator, R_1 and D_1. The three transistors and R_2 and R_3 form a high gain amplifier that is a very simple version of an operational amplifier – note the + and – signs in the circuit indicating the non-inverting and inverting inputs. The base of Q_2 is the non-inverting input, the base of Q_3 is the inverting input and the emitter of Q_1 is the output. R_2 is the collector resistor for Q_3 and R_3 sets the emitter currents of Q_2 and Q_3. The feedback network is the voltage divider, R_4 and R_5. Observe that this arrangement is identical to a standard non-inverting operational amplifier circuit and the output voltage would be Vref *(1 + R_4/R_5). Thus, if Vref were 5.1 volts and R_4 and R_5 were the same value then the output voltage would be 10.2 volts. The output capacitor, C_1, serves several purposes – it may be required for high frequency stability, it improves the transient response of the regulator to a rapidly changing load, it reduces the high frequency source impedance of the regulator, and it lowers electronic noise that might be superimposed on the output DC voltage. As in the circuit in Figure 1 the power dissipation of Q_1 may be significant so thermal design is required.

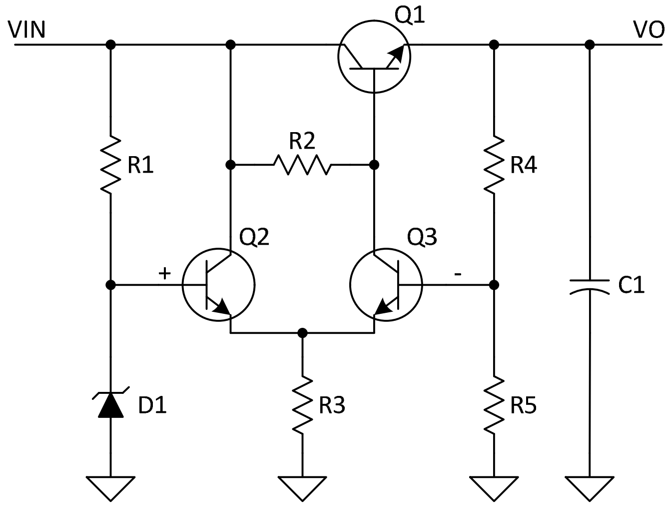

Figure 2: Simple series voltage regulator

The circuit in Figure 3 has higher voltage gain and can thus regulate more accurately. This is achieved by changing Q_1 to a PNP and operating it in the common-emitter mode rather than the common-collector mode in Figure 2.

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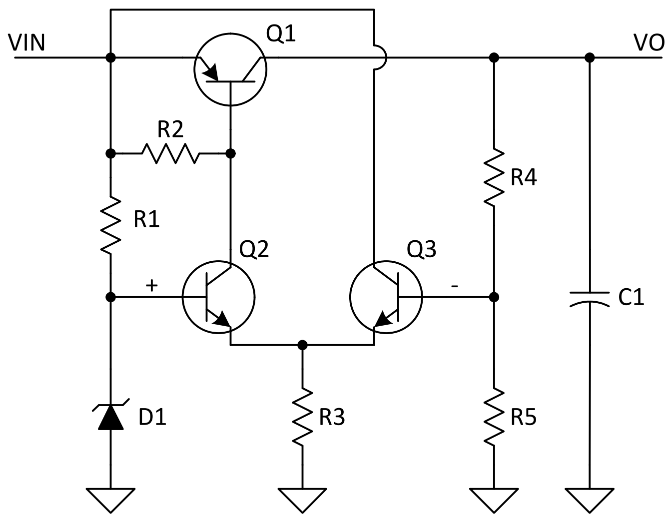

Figure 3: Simple series voltage regulator with higher gain

The regulators can be made to be adjustable by adding a potentiometer across the Zener diode as shown in Figure 6. However, for this to work well then R_3 must be replaced by a true current source and there must be a path to a negative voltage if output voltages near zero are required.

The circuits in Figures 1, 2 and 3 are about as simple as can be built. Refinements to the circuit would include:

- A more advanced circuit to make Vref extremely independent of V_{IN} and also to make Vref independent of temperature.
- A higher gain amplifier to hold the output voltage more accurately.
- A method to limit the fault current through Q_1 should there be a load fault.

Protection from load faults

One issue that can happen with any voltage regulator is a load fault – the load draws too much current or perhaps there is a short from V_O to ground. The excess current through Q_1 can cause it to fail either from damage or from excessive temperature rise. The solution is to incorporate a current limiter as shown in Figures 4 and 5. The two diodes in series forms a crude voltage reference of around 1.3 volts. There will be approximately 0.65 volts across the base-emitter junction of the transistor. As long as the load current is low enough so that the voltage drop across the series resistor (R_4 in Figure 4) then the voltage regulator operates normally and maintains the desired output voltage. When the load current is such that the voltage drop across R_4 is around 0.65 then the diodes begin conducting and shunt base drive current away from the transistor thus limiting the output current to be ~0.65/R_4.

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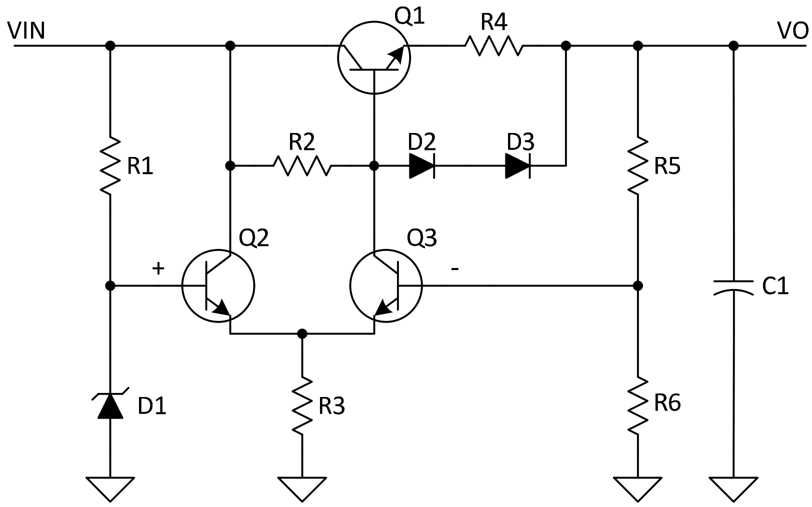

Figure 4: Current limiting function added to circuit in Figure 2

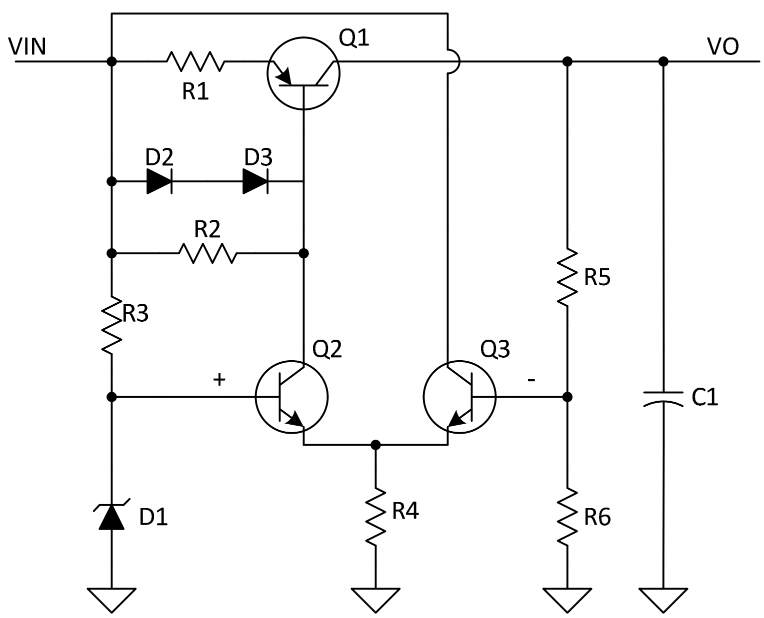

Figure 5: Current limiting function added to the circuit in Figure 3

Although the current is prevented from becoming excessive, the power dissipation of Q_1 can still exceed the thermal design since the worst case power dissipation is the input voltage multiplied by the limited current. The solution to that is known as fold-back limiting and involves additional circuitry (transistors) to shut off Q_1 until the load fault is cleared. When the load limit current is reached then the fold-back circuit trips and only a small current is applied to the load so that power dissipation of Q_1 is minimal. A periodic reset circuit might be used to un-trip the fold-back in an attempt to restore regulated voltage if/when the load fault clears. In some applications automatic reset could be a danger for equipment or people and shutoff is latched until manually reset when conditions are safe. Sample circuits are beyond the scope of this note but can easily be found on the Internet by Googling the phrase, "foldback current limiter".

Adjustable voltage regulators

An adjustable voltage regulator is an extension of the previous fixed voltage regulators. A potentiometer is used to vary the reference voltage. The circuit shown in Figure 6 is representative of a basic variable voltage power supply used in an electronic lab. The circuit features a higher gain amplifier for tighter control of the output voltage. The emitter resistor of the differential pair has also been replaced with a current sink for consistent operation over the entire output voltage range. The current sink must go to some negative voltage supply in order that the circuit control all the way down to zero volts. As shown the potentiometer can adjust the output voltage from zero to the Zener voltage multiplied by the non-inverting gain ($1 + R_9/R_{10}$). The circuit also features current limiting.

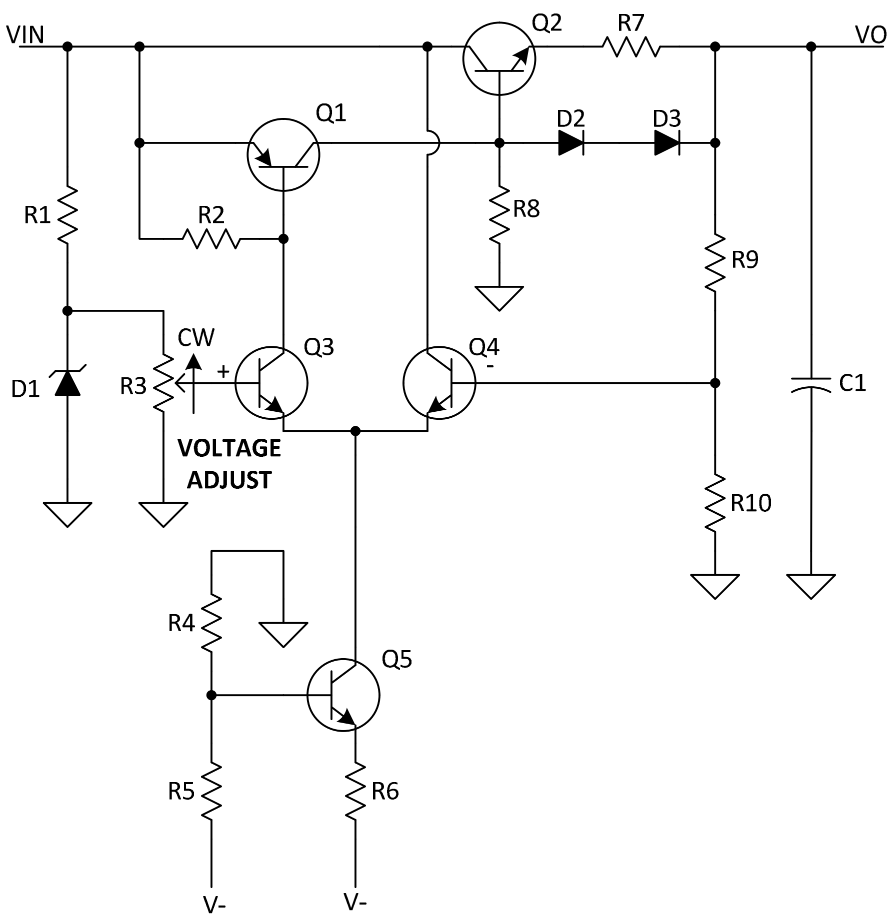

Figure 6: Basic variable voltage regulator

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Let's look at a typical lab power supply application using the circuit of Figure 6. We want an adjustable output voltage from 0 to ~20 volts at a current up to 0.5 amperes and with a current limit of ~0.6 amperes. This is very similar to one section of the lab power supply you use. The nominal unregulated input is ~26 volts with a source resistance of ~7 ohms. Design starts at the output and proceeds to the input. To keep the calculations simple in presentation we will use approximations and simplifications.

Determine R_7: The current limit resistor is calculated as 0.65 volts divided by 0.6 amperes which is 1.08 ohms. We will choose a **1.0 ohm** resistor for convenience.

Determine R_8: We will take the minimum beta of the power transistor, Q_2, to be 50. The next job is to determine the value for R_8. There is no absolute equation that gives us the value and there would be a spread of good values derived by different engineers. We generally want to make R_8 as small as practical consistent with not making it so small that it begins to dominate and thus limit the performance of the supply. What we have are guidelines that derive from detailed analysis of the circuit. One guideline is to choose R_8 so that the current through it about half the maximum base current into Q_2 at minimum beta when the output is at the maximum desired voltage and loaded to the maximum current. The maximum base current into Q_2 is 0.5/50 = 10 mA. The base voltage at the maximum output voltage is 20+0.65 = 20.65 volts. Thus R_8 computes to be 4,130 ohms. We will choose **4.7K** because is it a preferred standard value higher than calculated.

R_8 is shown connecting to ground. It could be connected to V- and its resistance increased to achieve the same current as previously discussed. Such a change would result in somewhat increased gain of the amplifier and some other improvements when the output voltage is set low.

Determine R_2: We next need to determine the maximum required current through Q_1. That will be the sum of the maximum base current of Q_1 plus the current through R_8 when the output is at the maximum voltage. That gives us 0.5/50 + 20.65/4,700 = 14.3 mA. The dynamic emitter resistance of Q_1 is 0.026/0.0143 = 1.82 ohms. The minimum input resistance at the base of Q_1 is 101*1.82 = 183 ohms. Considering that this is the minimum input resistance and that for lower output currents the resistance will be higher, a good choice for R_2 is in the range of double this value rounded up to the next higher preferred standard value. We will choose **R2 = 390 ohms**.

Determine Q_5 collector current: The current through R_2 is nominally 0.65/390 = 1.67 mA. The maximum base current to Q_3 is 14.3 mA/100 = 143 uA. Thus, the maximum current through the collector of Q_3 is 143 uA + 1.67 mA = 1.8 mA. The gain of the differential pair is a function of both the total current through Q_5 and the distribution of current between Q_3 and Q_4. The gain is highest when the currents are equal and approaches zero when the currents are highly different. Thus, we want to maximize the current but minimize the current difference. We also like to minimize the current without sacrificing too much gain. A reasonable compromise is to set the Q_5 current such that the amplifier gain is around 3 dB less than the ultimate for the maximum difference above.

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A rough guide is to set the current to 1.8 mA / (1 – 0.707) = **6.14 mA**. This is a general target we can freely deviate above or below.

Specify the reference voltage and potentiometer resistance and R_1: We will choose a temperature stable 5.00 voltage reference such as the LM336-5. We will also choose R_3 (the potentiometer) to be **5K** as that is a reasonable load of 1 mA for the voltage reference. Choosing an operating current of ~2 mA for the LM336-5 and adding 1mA for R_3 means that the current through R_1 is ~3 mA. We calculate R_1 as (26-5)/0.003 = 7,000 ohms. We will choose **R_1 = 6.8K**.

Determine R_9 and R_{10}: Considering that each end of the potentiometer is at a practically zero impedance point then the maximum source resistance from the potentiometer is at mid position where the source resistance would be on fourth of the total resistance or 1.25K. The non-inverting gain of the amplifier should be 4 so that when R_3 is at the maximum position that the output voltage of the regulator is 20 volts. Thus $(R_9/R_{10}) = 3$. For a good compromise in bias current compensation we would determine R_9 and R_{10} such that the ratio is the required three and that the source resistance of that voltage divider is around half the maximum source resistance of the potentiometer. This makes the bias current error theoretically zero when R_3 is at mid position. So we design for a nominal source resistance of 625 ohms. Calculation details are left to the student but the result is that **R_9 is 2.4K** and **R_{10} is 820 ohms**.

Determine C_1: The output capacitor, C_1 serves to maintain low output impedance at high frequencies where then gain of the amplifier is falling. There is no general calculation for the needed capacitance other than a general guideline that its impedance at several tens of kHz should be no more than a few ohms. For a specific application some details may be better known. Even then there is broad leeway in selecting the capacitor. As a general example we will say that the reactance at 10 kHz should be no more than 2 ohms. After a little calculation and rounding up to a standard value then C_1 is determined to be **10 uF**.

There is a tendency among some people to make C_1 as large as possible under the theory that more is better. That is very bad practice. The best value for C_1 is as large as it needs to be and no larger. Excessive values of C_1 will result in high charging currents reaching the current limit setpoint as the voltage adjust is increased and result in long voltage fall times if the load current is small when the voltage adjust is decreased since in that case the only discharge path is through R_9 and R_{10} – that time constant should generally be no more than a few tenths of a second maximum. In this case it is 32 milliseconds which is a not too large value. A real-world analogy of excess would be adding huge mass to a car to obtain very smooth speed. It works but think about the cost in terms of time to accelerate and stop and stress on the engine. The same is true for the voltage regulator.

The design of R_4, R_5, and R_6 for the 6.14 mA constant current sink will depend on what negative voltage is available. That calculation is straightforward. The base voltage of Q_5 should be at least 2 volts below the minimum setting of the potentiometer, R_3. Otherwise the base-collector junction of Q_5 will be insufficiently reverse biased.

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Determine worst case power dissipation of Q_2: The worst case power dissipation of Q_2 occurs when the load voltage is practically zero volts and the current limit is through it. For this case the input voltage would be 26-0.6*7 = 21.8 (remember the ~7 ohm source resistance). The voltage at the emitter would be ~0.65 because of the voltage drop across R_7. The Q_2 power dissipation is then (21.8 – 0.65)*0.6 = **<u>12.7 watts</u>**.

Determine the amplifier gain: Calculating the gain of the amplifier is a bit tricky as it depends on load conditions. A representative situation will be presented. Approximations to exact calculations will be used for simpler presentation. There is no point in trying to calculate an exact answer as it varies a lot with operating conditions. All we need is a representative answer. We will analyze the specific design case.

The emitter current of Q_3 is (101/100)*1.8 mA = 1.818 mA and the dynamic emitter resistance of Q_3 is 0.026/0.001818 = 14.3 ohms. The emitter current of Q_4 is 6.14 mA – 1.818 mA = 4.322 mA. The dynamic emitter resistance of Q_4 is 0.026/0.004322 = 6.02 ohms. The total dynamic emitter resistance is the sum or 20.32 ohms.

The input resistance of Q_1 has already been calculated to be 183 ohms. The net collector load resistance of Q_3 is then 183 ohms in parallel with 390 ohms or 125 ohms.

The voltage gain of the differential pair, Q_3, and Q_4, is then (100/101)*125/20.32 = **<u>6.09</u>**.

For the 20 volt, 0.5 ampere case the load resistance is 40 ohms and the input resistance of the base of Q_2 is 51*40 = 2,040 ohms. The net load resistance of Q_1 is the parallel combination of 4,700 and 2,040 which is 1,423 ohms. The voltage gain of Q_1 is (100/101)*1,423/1.82 = **<u>774</u>**.

The total gain of the amplifier is 6.09*774 = **<u>4,714</u>**. This is a respectable amount of gain although professional amplifiers would have features to extend that by at least an order of magnitude.

Calculate the output resistance of the regulator: The open-loop output resistance of the voltage regulator is approximately R_8/51 + R_7 = 4,700/51 + 1 = 93 ohms. The closed-loop output resistance is the open-loop value multiplied by the closed-loop non-inverting gain and divided by the open-loop gain. This is 93*4/4,714 = **<u>0.079 ohms</u>**. This means that for the example case the change in output voltage from 0 to 0.5 amperes load would be 0.039 volts. Thus, if the no-load output voltage was set to 20.00 then the fully loaded output voltage would be 19.96.

Not bad but more complete professional power supplies do much better. A professional lab supply would add some improvements to obtain higher gain and be insensitive to temperature drift in Q_3 and Q_4. Also, this amplifier has a fairly high input offset voltage – probably in the low tens of millivolts. The bias current and offset current are also relatively high. However, this amplifier can be expected to perform a fair job for the application.

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Three-terminal IC voltage regulators

Because voltage regulators are so often needed, a number of manufacturers sell monolithic voltage regulators in three terminal packages. Usually, the only external parts required are input and output bypass capacitors per the applications notes. These capacitors are generally required to be located as close as practical to the terminals and must be a specific value and type in order that the regulator not oscillate. Always consult the manufacturer's data sheet and application notes. The internal circuitry is a series regulator just like those discussed but with some premium features for top performance.

There are two types of three-terminal regulators, fixed voltage and adjustable voltage. The fixed voltage types have all of the internal circuitry necessary and are available in common voltages of 5, 8, 12, 15, 18, and 24 among other voltages. An example circuit is shown in Figure 7. The user should be aware that if the load current is more than a very small amount that the package will have to dissipate significant heat and thermal design is necessary. Some common part numbers are: LM7805 (+5 volt) and LM7812 (+12 volt). For negative output voltages with negative input voltages some common parts are the LM7905 (-5 volt) and LM7912 (-12 volt).

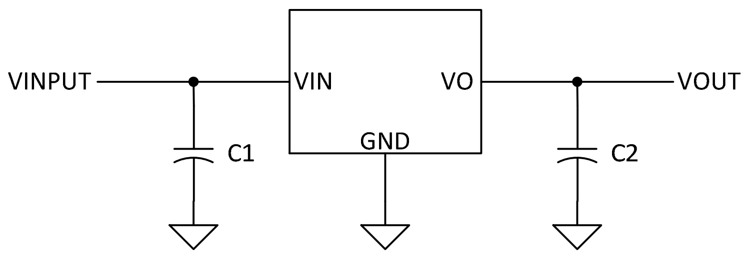

Figure 7: Three-terminal voltage regulator

An adjustable voltage regulator is used when the needed voltage is not one of the standard values available in fixed types. A common part number is the LM337 and is shown in Figure 8. In operation the internal circuitry maintains a constant voltage known as V_{REF} (typically 1.25) between the Vadj and V_O terminals. That forms a constant current through R_2 since the voltage across it is fixed. Generally, R_2 must be small enough so that the constant current is at least 10 milliamperes in order for the regulator to operate properly – this data is in the application notes which should always be consulted. There is a small current leaving the Vadj terminal and the constant current should be very large in comparison to minimize errors. With a constant current through R_2 then there is a constant current through R_1 and the output voltage is simply the voltage across R_1 plus the internal reference voltage of the regulator. This can be expressed as an equation as

$$V_O = V_{REF}\left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

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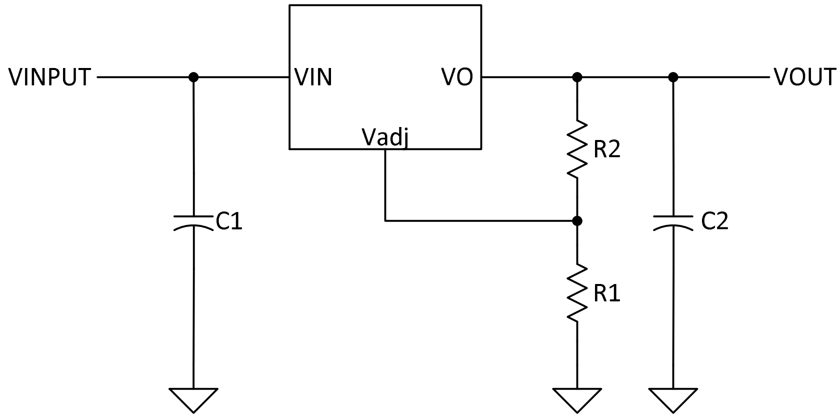

Figure 8: Three-terminal adjustable voltage regulator

To make the output voltage variable a wire-wound potentiometer or rheostat can be used for R_1. Carbon composition or film type potentiometers do not work well in this application since the wiper must take significant current which causes early failure.

Homework

1. In Figure 2 or Figure 3 if the reference voltage were 2.5 volts and R_4 was 10 K and R_5 was 3.33 K, what would the expected output voltage be? (answer: 10 volts)

2. In Figure 1 if V_{IN} were 15 volts and V_O was 10 volts and the load current was 50 millamperes, what would the power dissipation of Q_1 be? (answer: 0.25 watts)

3. In Figure 8 if Vref is 1.25 volts and R_2 is 100 ohms and R_1 is 620 ohms, what is the output voltage? (answer: 9.0 volts)

4. In Figure 8 if Vref is 1.25 volts, and R_2 is 100 ohms, what must the value of R_1 be so that the output voltage is 6.125 volts? (answer: 390 ohms)