Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

by Kenneth A. Kuhn
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Introduction

This article discusses the process for determining the optimum bias conditions for a common-emitter amplifier operating without negative feedback in order to maximize the linear output signal swing. This process is quite complicated but the results are simple to apply. The full derivation is shown to illustrate that one should not shy away from complicated algebra. The results are often much simpler and very useful. The reference circuit is shown in Figure 1.

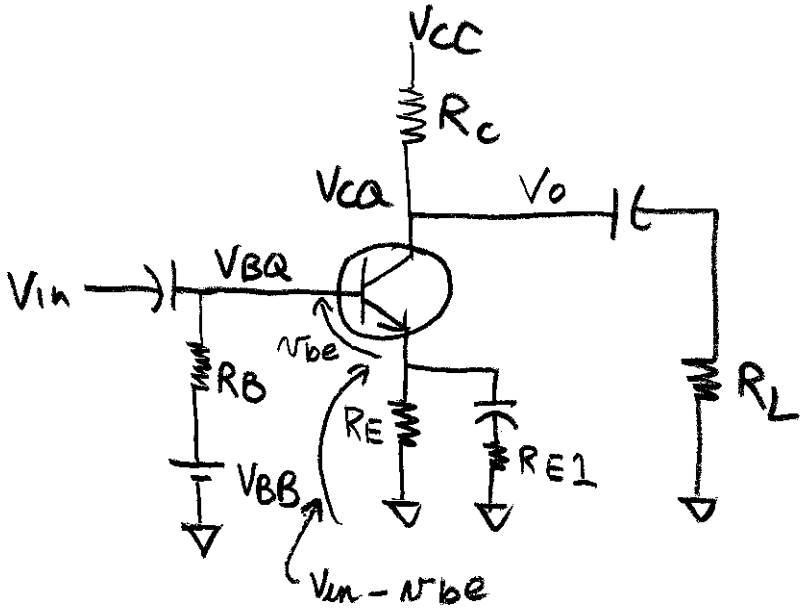

Figure 1: Common-emitter Amplifier

Summary of non-linear effects

A bipolar junction transistor is a non-linear device. Output signal swing is only linear-ish over a small region of operating current. There are a number of factors that contribute to non-linear operation of the transistor including:

- The dynamic emitter resistance, re, varies with signal amplitude. Thus, the amplifier gain varies dynamically with signal amplitude.
- Beta varies with collector current.
- The collector output resistance, ro, varies with collector current.

The most dominate factor is the variation of the dynamic emitter resistance, re, with signal amplitude and this article focuses on that aspect.

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

As discussed in the article, *Distortion in BJT Amplifiers*, the modulation of the collector or emitter current by the applied signal is a function of how much signal voltage, vbe, appears across the base-emitter junction. k is defined as the ratio of the peak-peak signal, vbe, across the base-emitter junction to the thermal voltage, V_T (26 mV at room temperature). k is also the ratio of peak-peak collector or emitter current to the quiescent value. The two definitions are equivalent. The following is a summary of the results from that article.

k	vbe pp	iepp / I_{EQ}	Distortion	Comment
2	52 mVpp	2	25 %	Severe
1	26 mVpp	1	12.5 %	High
0.5	13 mVpp	0.5	6.25 %	Moderate
0.2	5.2 mVpp	0.2	2.5 %	Fair
0.1	2.6 mVpp	0.1	1.25 %	Low
0.05	1.3 mVpp	0.05	0.625 %	Very low

Table 1: Summary of Distortion as a function of k

This distortion is only a function of the degree of modulation of the emitter current and is independent of the actual value for I_{EQ}. The above table indicates that if the signal voltage across the base-emitter junction is 26 mVpp (i.e. k = 1) then the (theoretical linear) peak-peak value of either emitter or collector current will be equal in magnitude to the quiescent and that the resulting distortion is in the high range of around 12%. For lower distortion the applied signal must be smaller. Note that this is the signal across the base-emitter junction and not necessarily the total input voltage (See Figure 1) since any external emitter impedance ($R_E \parallel R_{E1}$) will have a portion of the input signal voltage across it. A simple rule for signal voltages less than about 20 mVpp across the base-emitter junction is that the distortion in percent is the signal voltage multiplied by 481. A k value of 1.0 is normally the absolute maximum value we consider for open-loop amplifiers. For open-loop amplifiers we typically we design for k values between 0.2 and 1 in order to obtain low distortion. A k value of 0.2 is in the range of impractically low – if low distortion is required then we always plan for negative feedback. For the closed loop case, negative feedback is used to reduce distortion and k values between 1 and 2 are common. Negative feedback significantly increases the linear output signal swing.

The following figures illustrate examples of the optimum bias point for different values of k. In all cases the amplifier is powered from +15 volts and a V_{CB}min (the difference between the negative peak of the collector signal and the positive peak of the base signal) of 2 volts was used in the design. The amplifier has a low gain of 8 (so that the base signal voltage is visible in the plots) and has no load connected. The signal amplitudes are the maximum values based on the k value shown. Obviously, the distortion will be less if lower amplitudes are used. An undistorted output sine wave is shown for reference. Distortion is the difference between the actual waveform and the reference waveform.

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

Except for Figures 2 and 6 the optimum V_{BQ} and V_{CQ} are shown for each example – to maximize the signal amplitude for the example distortion. Observe that as k is lowered, that the optimum V_{CQ} is also lowered in order to increase the collector current which in turn maximizes the output signal. The value for the optimum V_{BQ} varies but is not as obvious.

In the last case, Figure 6, a V_{CQ} above the optimum is used and the output amplitude is less (by a factor of one-half) than for the optimum case shown in Figure 5. This is why we are going through the process to determine the optimum V_{CQ}. For these two figures it might seem logical that more output signal could be obtained by increasing the input signal. That is true – but the resulting distortion is increasing too – as if a higher k value was used but with less than optimum bias conditions. What is shown in all the figures is the maximum output that can be obtained for a given level of distortion.

In all of the following figures the V_{CC} line is shown for reference as an aid to understanding the whole bias structure.

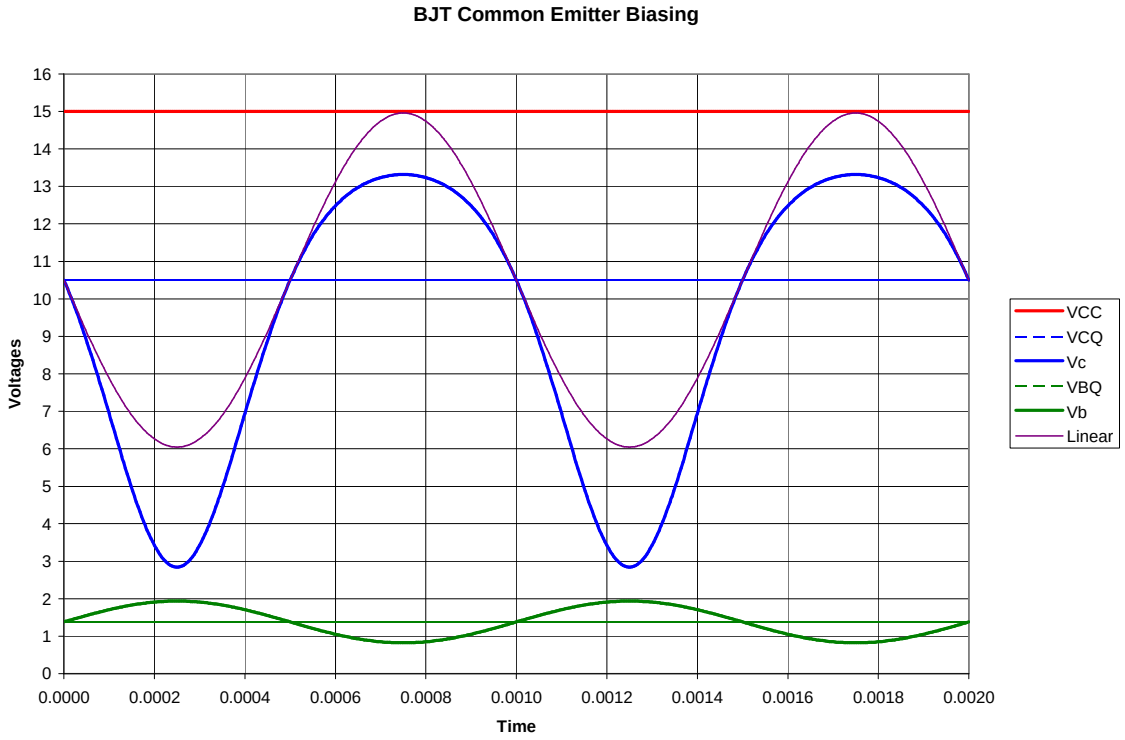

Figure 2: Severe distortion with k=2 – gain varies significantly with amplitude

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

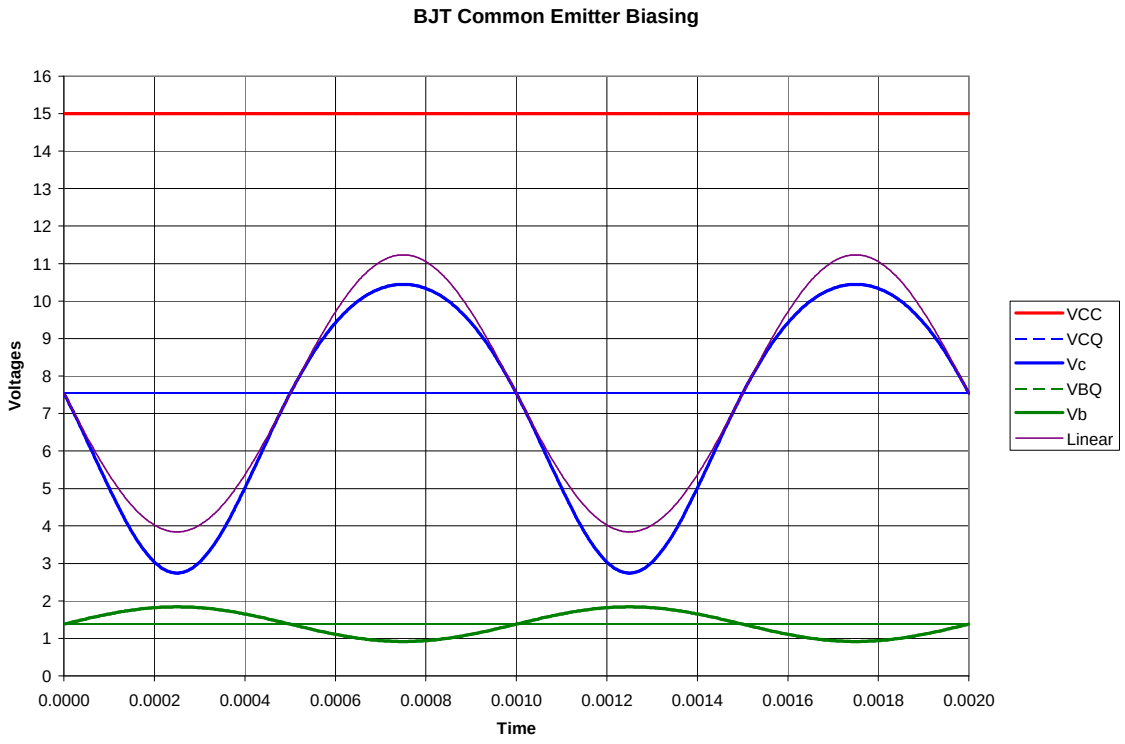

Figure 3: High distortion with k=1

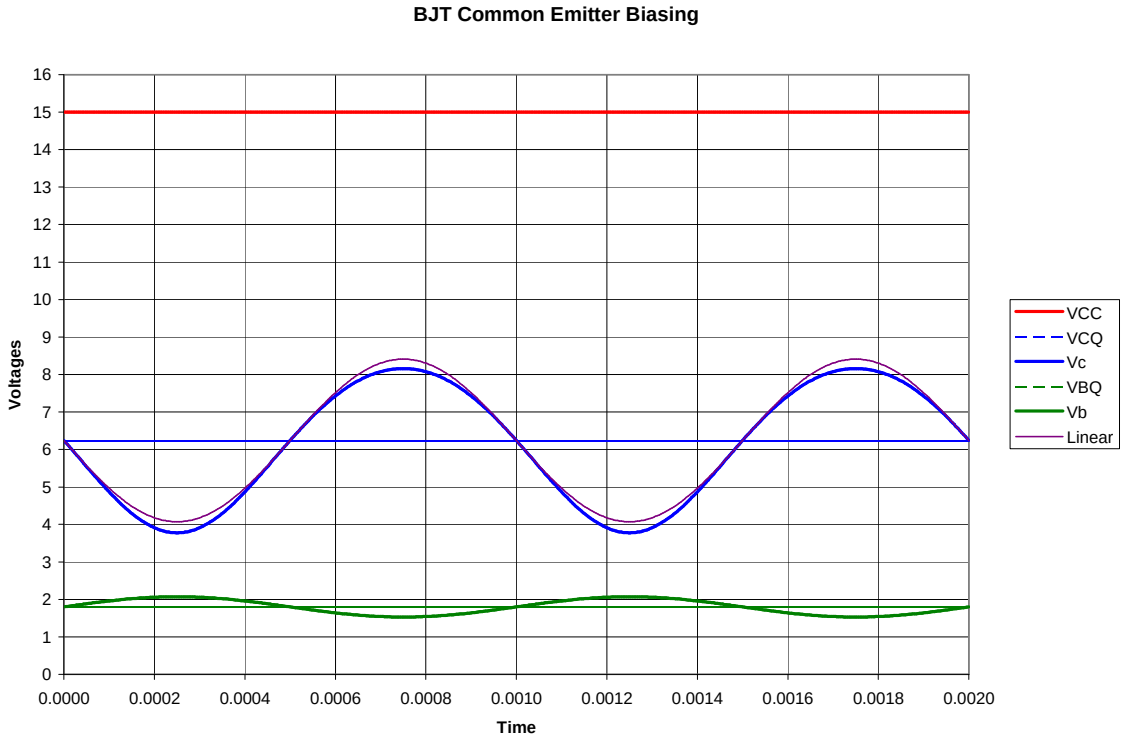

Figure 4: Moderate distortion with k=0.5

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

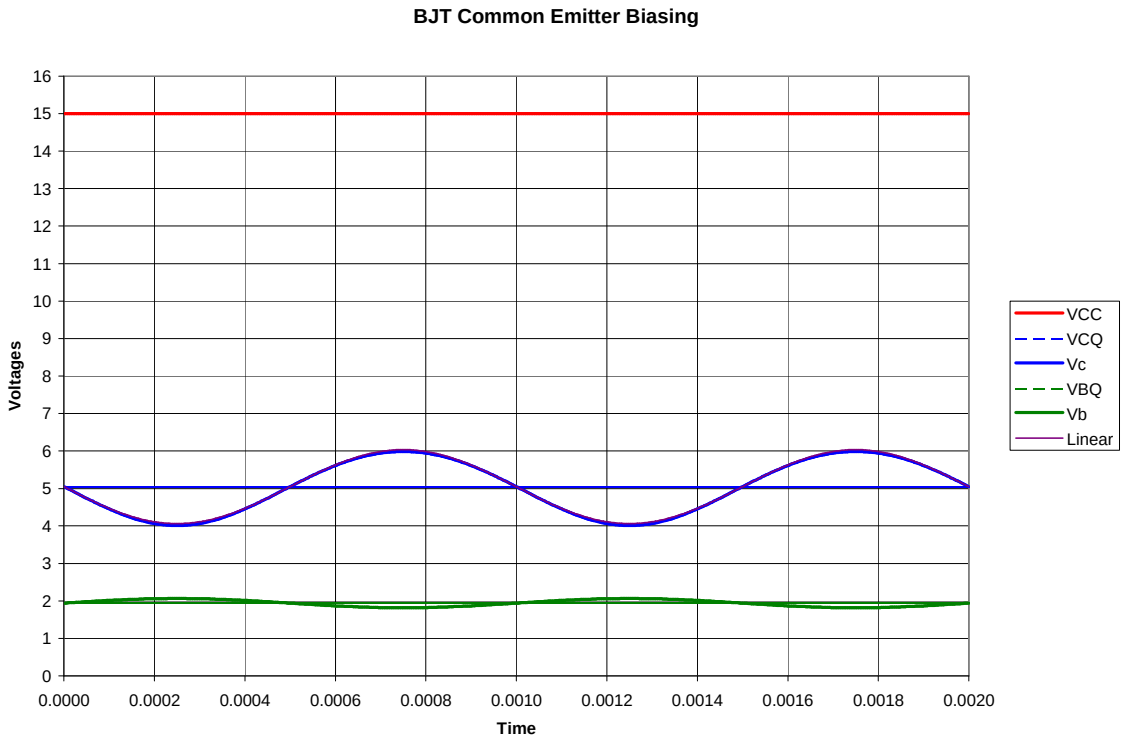

Figure 5: Low distortion with k=0.2

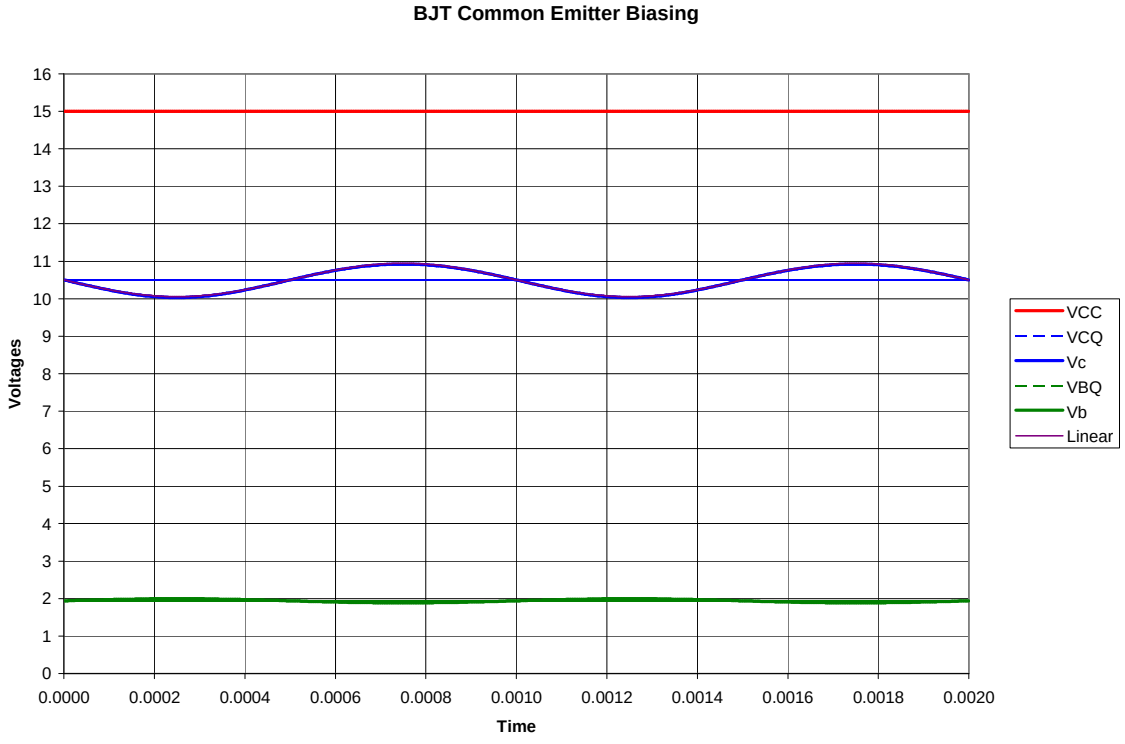

Figure 6: As previously with k=0.2 but higher V_{CQ} resulting in lower linear amplitude

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

Development of VCQopt

From Table 1 the peak-peak collector current for a given value of k is

$$I_C pp = k * I_{CQ} \qquad \text{Eq. 1}$$

This ignores non-linear effects since the intent here is to use a k value less than 1.

From Ohm's law, the maximum output signal voltage at the collector of the transistor is

$$Voppmax = k * I_{CQ} * R_C||R_L \qquad \text{Eq. 2}$$

Noting that I_{CQ} is the voltage across R_C divided by R_C, Equation 2 can be written as

$$Voppmax = \frac{k * (V_{CC} - V_{CQ}) * R_C||R_L}{R_C} \qquad \text{Eq. 3}$$

which simplifies to

$$Voppmax = \frac{k * (V_{CC} - V_{CQ})}{W + 1} \qquad \text{Eq. 4}$$

where W represents R_C/R_L for convenience in the following mathematics.

Equation 4 indicates that for maximum linear output signal swing that V_{CQ} should be as low as possible. However, V_{CQ} must be sufficiently above V_{BQ} in order to accommodate negative voltage swing. The conclusion here is that for a given V_{BQ} there is an optimum V_{CQ} (as low as possible) that maximizes linear output signal swing. The following mathematics derives that optimum. This is best illustrated graphically as follows.

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

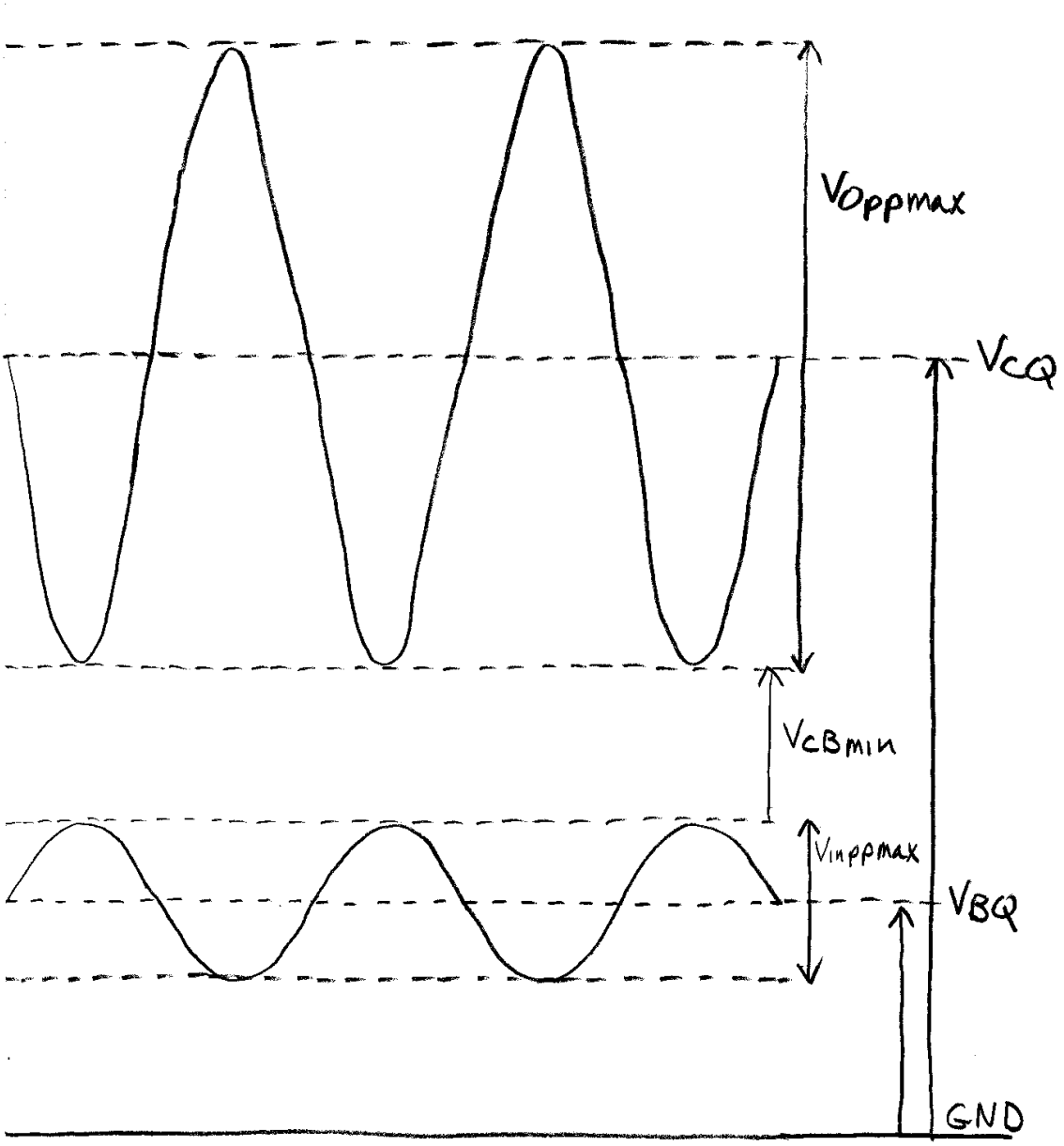

Figure 7: Signal levels

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

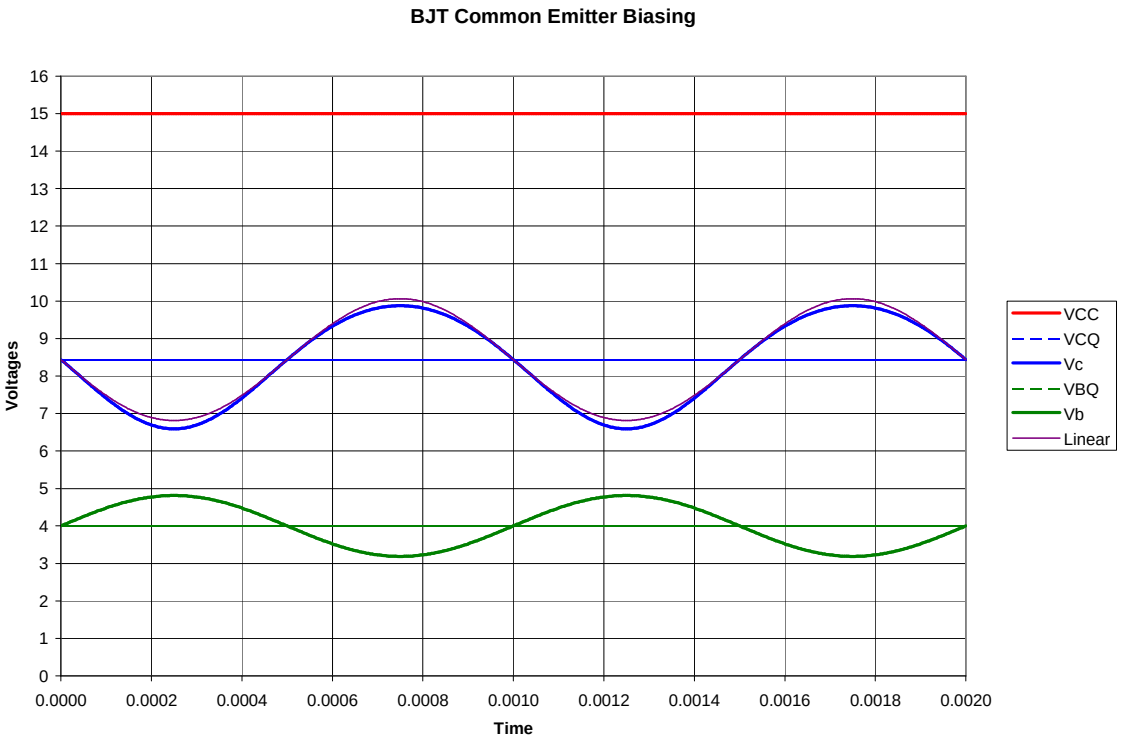

Figure 8: BJT low-gain biasing for maximum signal swing showing optimum bias

It must be remembered that the output signal from a common-emitter amplifier is inverted relative to the input. This means that as the input signal is rising the output signal is falling as shown in Figures 7 and 8. For the case of high gain amplifiers the input signal is very small. For the special case where the amplifier gain is low (sometimes as low as 1 or 2) the effect is significant and that requires that V_{CQ} be a higher voltage in order that a collision (i.e. a forward bias condition of the base-collector junction) does not occur between input and output.

It is desirable that there be a minimum reverse bias voltage, V_{CB}min, between the base and the collector. Stated differently, there should be a minimum voltage between the positive peak of the input signal and the corresponding negative peak of the output signal. Typically V_{CB}min is chosen to be in the 1 to 2 volt range but at the extreme could be as low as 0 for low frequency amplifiers. Because the capacitance between the base and collector junctions is inversely related to the reverse bias voltage then for high frequency amplifiers V_{CB}min might be chosen to be greater than 4 volts – but that is a topic of another article. For now, we will allow that there is some target value of V_{CB}min and include that in the derivation for optimum V_{CQ}. In short, as long as the capacitance between the base and collector is not an issue then V_{CB}min can approach zero volts. There is a larger minimum when signal frequencies are high enough so that base-collector capacitance is non-insignificant.

Stated in words, the optimum value for V_{CQ} is the sum of the given V_{BQ} plus the maximum positive peak magnitude for linearity of the input signal plus V_{CB}min plus the

magnitude of the maximum negative peak magnitude of the output signal. This can be seen in Figure 7 and also in Figure 8 which illustrates a low-gain example of two with optimum bias conditions. For high gain cases we can ignore the peak magnitude of the input signal as that is very small.

Expressed mathematically,

$$V_{CQ}opt = V_{BQ} + \frac{k * (V_{CC} - V_{CQ})}{2 * Avl * (W + 1)} + V_{CB}min + \frac{k * (V_{CC} - V_{CQ})}{2 * (W + 1)} \qquad \text{Eq. 5}$$

maximum input signal peak maximum output signal peak

where Avl is the magnitude of the loaded gain of the amplifier. Remember that $W = R_C/R_L$.

Equation 5 simplifies to

$$\mathbf{V_{CQ}opt = \frac{2 * (W + 1) * (V_{BQ} + V_{CB}min) + k * V_{CC} * (1 + 1/Avl)}{2 * (W + 1) + k * (1 + 1/Avl)}} \qquad \mathbf{Eq.\ 6}$$

The value of V_{BQ} in Equation 6 is the actual value for the circuit and may or may not be the optimum but that does not matter here. V_{CQ}opt is the best that can be achieved for the given V_{BQ}. The next section will discuss how to optimize V_{BQ}.

Equation 6 has a number of variables and that creates difficulty in stating some general conclusions. One fact should be very clear – that V_{CQ}opt is somewhere between V_{BQ} + V_{CB}min and V_{CC}. Stated differently, V_{CQ}opt will be just enough higher (i.e. much below V_{CC}) than V_{BQ} + V_{CB}min to maximize the linear output signal swing. We note that the typical range of W is 0.5 for large loaded output signal swing to 2 for high loaded gain. As stated previously, k is typically in the range of 0.2 to 1. The effect of the loaded stage gain, Avl, diminishes as gain is large.

Table of V_{CQ}opt for V_{BQ} = 1.5 volts, V_{CB}min = 2 volts, V_{CC} = 15 volts, and W = 1

Avl	k = 0.2	k = 0.5	k = 1.0
5	4.15	5.00	6.15
10	4.10	4.89	5.98
20	4.07	4.83	5.89
50	4.06	4.80	5.84

Table 2

From Table 2 it can be observed that Avl has only a very small effect and can generally be ignored except for the special case of values in the low signal digits. The dominant factor is k. Because lower values of k lead to higher collector currents (with everything else the same) then the maximum linear output signal swing is higher as k is reduced.

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

Development of VBQopt

As discussed previously, the emitter current variation in response to the maximum peak-peak input signal divided by the quiescent emitter current is k. The following relates this current variation to the input voltage. Note that Vbp is Vinppmax/2 – i.e. the peak input signal voltage. This is a shorthand notation for convenience so that Eq. 7 does not appear unnecessarily complicated. The peak-peak emitter current is the difference between the maximum and minimum values so we can write from the definition of k

$$k = \frac{I_E max - I_E min}{I_{EQ}} = \frac{(V_{BQ} - V_{BE} + Vbp) / R_E \; - \; (V_{BQ} - V_{BE} - Vbp) / R_E}{(V_{BQ} - V_{BE}) / R_E} \qquad \text{Eq. 7}$$

Equation 7 simplifies to

$$k = \frac{2 * Vbp}{V_{BQ} - V_{BE}} = \frac{Vinppmax}{V_{BQ} - V_{BE}} \qquad \text{Eq. 8}$$

Equation 8 can be solved for V_{BQ} as follows

$$V_{BQ} = Vinppmax / k + V_{BE} \qquad \text{Eq. 9}$$

By dividing the maximum peak-peak output signal by Avl we obtain the maximum peak-peak input signal as follows making use of Equation 4.

$$Vinppmax = \frac{k * (V_{CC} - V_{CQ})}{Avl * (W + 1)} \qquad \text{Eq. 10}$$

Substituting Eq. 10 into Equation 9 gives

$$V_{BQ} = \frac{V_{CC} - V_{CQ}}{Avl * (W + 1)} + V_{BE} \qquad \text{Eq. 11}$$

From Equation 11, note that the optimum value for V_{BQ} approaches V_{BE} for very large Avl. In reality we will use a value of V_{BQ} consistent with bias temperature stability requirements. Observe also that Equation 11 indicates that the V_{BQ} must increase if Avl is relatively low. We are now at a point where in order to solve for the optimum V_{BQ} we need the optimum V_{CQ} – but we can not know that value until we have V_{BQ}. We need a way out of this circle to directly obtain the optimum V_{BQ}. The following mathematics will do this. Although the algebra becomes rather tortuous the end result is not too bad. That is typical of design mathematics. Equation 6 below is copied here for convenience from the earlier result for V_{CQ}opt.

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

$$V_{CQ}opt = \frac{2 * (W + 1) * (V_{BQ} + V_{CB}min) + k * V_{CC} * (1 + 1/Avl)}{2 * (W + 1) + k * (1 + 1/Avl)} \qquad \text{(Eq. 6)}$$

We now substitute Equation 6 into Equation 11. This equation looks bad and the initial algebra appears to become worse but we are compelled to solve this equation because the only unknown is VBQ – the value that we are seeking.

$$V_{BQ} = V_{CC} - \frac{2 * (W + 1) * (V_{BQ} + V_{CB}min) + k * V_{CC} * (1 + 1/Avl)}{2 * (W + 1) + k * (1 + 1/Avl)} \Big/ Avl * (W + 1) + V_{BE} \qquad \text{Eq. 12}$$

The next step just breaks Equation 12 into its main parts.

$$V_{BQ} = \frac{V_{CC}}{Avl * (W + 1)} - \frac{2 * (W + 1) * (V_{BQ} + V_{CB}min) + k * V_{CC} * (1 + 1/Avl)}{2 * (W + 1) + k * (1 + 1/Avl)} + V_{BE} \qquad \text{Eq. 13}$$

Now we combine the V_{BQ} terms.

$$V_{BQ} * \left[1 + \frac{2 * (W + 1)}{Avl * (W + 1) * [2 * (W + 1) + k * (1 + 1/Avl)]} \right]$$

$$= \frac{V_{CC}}{Avl * (W + 1)} - \frac{2 * (W + 1) * V_{CB}min + k * V_{CC} * (1 + 1/Avl)}{Avl * (W + 1) * [2 * (W+1) + k * (1 + 1/Avl)]} + V_{BE} \qquad \text{Eq. 14}$$

Now we make common denominators for both sides.

$$V_{BQ} * \left[\frac{[Avl *[2 * (W + 1) + k * (1 + 1/Avl)] + 2]}{[Avl *[2 * (W + 1) + k * (1 + 1/Avl)]]} \right]$$

$$= \frac{V_{CC}*[2*(W+1) + k*(1+1/Avl)] - 2*(W+1)*V_{CB}min - k*V_{CC}*(1+1/Avl) + V_{BE} *Avl*(W+1)*[2*(W+1) + k*(1+1/Avl)]}{Avl *(W+1)*[2*(W+1) + k*(1+1/Avl)]}$$

Eq. 15

The denominators cancel and with further simplification we obtain the following.

$$V_{BQ} = \frac{2 * (V_{CC} - V_{CB}min) + V_{BE} * (Avl * [2 * (W + 1) + k * (1 + 1/Avl)])}{Avl * [2 * (W + 1) + k * (1 + 1/Avl)] + 2} \qquad \text{Eq. 16}$$

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

The final result after some simplification (an exercise for the student) is shown below.

$$V_{BQ}opt = \frac{V_{BE} + \dfrac{2 * (V_{CC} - V_{CB}min)}{Avl * (W + 1 + k/2) + k/2}}{1 + \dfrac{1}{Avl * (W + 1 + k/2) + k/2}} \qquad \textbf{Eq. 17}$$

Remember from before that $W = R_C / R_L$. Equation 17 provides the optimum V_{BQ} in order to maximize the output signal swing for a given value of k. For high gain amplifiers it is likely that $V_{BQ}opt$ will be below the minimum V_{BQ} for a specified bias stability with temperature. We will always use the larger of the two calculations for V_{BQ}. Then we use the chosen V_{BQ} and Equation 6 to calculate the optimum V_{CQ}. With these two values known then we can complete the design of the amplifier. The following is a summary algorithm to follow.

1. Specify R_L and choose an appropriate R_C in relation to R_L.
2. Calculate $W = R_C/R_L$.
3. Specify V_{CC} and the desired V_{CB}min.
4. Specify Avl. This can be Av if $R_L >> R_C$.
5. Specify the desired value of k for the maximum level of tolerable distortion.
6. Calculate (R_B/R_E)max for the specified beta stability factor, K_B, for the beta range of the transistor – refer to the article on bias design. Also calculate the nominal beta.
7. Calculate V_{BQ}opt from Equation 17.
8. Calculate V_{BQ}min for the specified temperature stability factor, K_T, for the specified operating temperature range – refer to the article on bias design. Also calculate the nominal V_{BE}.
9. Use the larger V_{BQ} from the above.
10. Calculate V_{CQ}opt by substituting the chosen V_{BQ} into Equation 6.
11. Complete the bias design by determining R_E, and the base bias resistors.
12. Compute R_{E1} for the desired Avl.

An example of this algorithm begins on the next page.

Optimum V_{BQ} and V_{CQ} Bias Conditions for Maximum Linear Output for the Common-Emitter Amplifier

Example Design Problem: Design a common-emitter amplifier with an Avl of 20 (see note below) that will drive a load resistance of 2000 ohms. The output signal swing should be as large as possible for no more than 5% distortion at full output. The available power supply voltage is 15 volts. The operation temperature is 0 to 70 C and the bias stability factor, K_T, over this temperature range should be no more than 1.1. The beta range for the transistor is 100 to 240 and the bias stability factor, K_B, should be no more than 1.1. Use a V_{CB}min of 2 volts. Use V_{BE} = 0.65 volts @ 25 C with a temperature coefficient of -2 mV/C.

Note: We know this is really -20 because of phase inversion but we are using magnitude rather than vectors here.

Step 1: Since large output signal swing is important we will choose an R_C that is smaller than RL. Using previous guidelines a good value for R_C is one-half R_L or 1000 ohms.

Step 2: W = 1000 / 2000 = 0.5

Step 3: V_{CC} = 15 volts and V_{CB}min = 2 volts.

Step 4: Avl is 20.

Step 5: Referring to Table 1, k should be 0.5 for 5% maximum distortion.

Step 6: From the bias design article,
$[(R_B/R_E) = 1.1 * (241/240) – 101/100] / (1/100 – 1.1/240) = 17.5$

The nominal beta is sqrt(100 * 240) = 155

Step 7: Using Equation 17, V_{BQ}opt = 1.35 volts.

Step 8: At 0 C, V_{BE} will be 0.65 + (25 – 0) * 0.002 = 0.700 volts
At 70 C, V_{BE} will be 0.65 – (70 – 25) * 0.002 = 0.560 volts
From the bias design article, the minimum value of V_{BB} for the given temperature stability is
V_{BB}min = [(1.1 * 0.700) – 0.560] / (1.1 – 1) = 2.1 volts

The nominal V_{BE} is (0.56 + 0.700) / 2 = 0.630

Thus, V_{BQ}min = [2.1 + 0.630*17.5/155] / [1 + 17.5/155] = 1.95 volts

Step 9: The larger of the two calculations for V_{BQ} is 1.95 volts so that is what we will use.

Step 10: Using Equation 6, V_{CQ}opt = 5.6 volts

Step 11: We determine R_E by noting that I_{CQ} = (15 – 5.6) / 1000 = 9.4 mA

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I_{EQ} = (156/155) * 9.4 mA = 9.46 mA

$V_{EQ} = V_{BQ} – V_{BE}nom = 1.95 – 0.630 = 1.32$ volts

$R_E = V_{EQ} / I_{EQ} = 1.32 / 0.00946 = 139.5$ ohms which we round to the standard value of 130 ohms.

Since we still want the same I_{EQ} then we compute the new V_{EQ} as 0.00946 * 130 = 1.23 volts. The new V_{BQ} is 1.23 + 0.63 = 1.86 volts. Yes, this is less than the minimum calculated earlier but we are in the round-off zone – our calculations are only good approximations – we do not worry about small fractions of a volt – it is not going to make any difference to us in the final result.

We calculate R_B as 17.5 * 130 = 2,275 ohms.

Using the bias design article we calculate the required VBB as

$V_{BB} = 1.86 + (1.86 – 0.630) * 17.5) / 155 = 2.0$ volts.

$V_{CC}/V_{BB} = 15 / 2.0 = 7.5$

$(R_{B1}/R_{B2}) = 7.5 – 1 = 6.5$

R_{B1} = 2,275 * 7.5 = 17063 ohms which we round to the standard value of 18K.

R_{B2} = 18K / 6.5 = 2.77K which we round to the standard value of 2.7K.

Step 12: Now we calculate the required value for R_{E1} for the specified gain using notes from the article on designing AC gain.

re = 0.026 / 0.00946 = 2.75 ohms

$R_C \parallel R_L = 1000 \parallel 2000 = 667$ ohms

We note that $20 = Avl = (B/B+1) * R_C \parallel R_L / (re + R_E \parallel R_{E1})$

$re + R_E \parallel R_{E1} = (155/156) * 667 / 20 = 33.14$ ohms

Thus, $R_E \parallel R_{E1} = 33.14 – 2.75 = 30.39$ ohms

Thus, $R_{E1} = 130 * 30.39 / (130 – 30.39) = 39.66$ ohms which we round to the standard value of 39 ohms.