EE351 Test 2 Build								
1. JFET common-source amplifier								
IDSS	**VP**	**VDD**	**R1**	**R2**	**R3**	**RL**		
0.008	***-3.0***	***15***	***1,000,000***	***1,000***	***100***	***2,000***		
			RG	RD	RS			
3.000	**VK**	**0.005386**	**ID**	**0.004376**	**gm**	**1,000,000**	**Rin**	
1,125	**VR**	**9.61**	**VD**	**-4.38**	**Av**	**-2.92**	**Avl**	
0.533	**X**			**0.667**	**vd**	**1000.00**	**Ro**	
2. Design RS for bias condition								
IDSS	**VP**	**VDD**	**R1**	**ID**				
0.010	***-4.0***	***20***	***1,000,000***	***0.007***				
-0.65	**VGS required**							
93	**RS calculated**							
3. Design VGG for bias condition and analyze amplifier								
IDSS	**VP**	**VDD**	**ID**	**R2**	**R3**	**R4**	**RL**	
0.015	***-4.5***	***20***	***0.010***	***750***	***1,000,000***	***470***	***1,000***	
					RG	RS		
4.70	**VS**			**0.005443**	**gm**			
-0.83	**VGS required**			**1,000,000**	**Rin**			
3.87	**VGG calculated**			**132**	**Ro**			
0.005166	**Amperes through R2**			**0.719**	**Av**			
16.13	**Voltage drop across R1**			**0.635**	**Avl**			
3,122	**R1 calculated**							
4. Analyze multistage amplifier								
Beta	**VBE**	**VCC**	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**
150	***0.65***	***12***	***2,200***	***390***	***2,700***	***18,000***	***1,000***	***390***
			RB1	RE1	RC2	RB2	RC1	RE2
10.69	VBB1	15.95	re1		10.64	re2		
1,960	RB1	2,408	rbt1		1,606	rbt2		
-0.001630	IE1	-62	Av1		-252	Av2		
-0.001619	IC1				0.616	interstage voltage division		
1.62	VBB2	**1,081**	**Rin**					
0.002444	IE2	**9,678**	**Av**		1.31	VCC-VBB1		
0.002428	IC2	**2,700**	**Ro**					
5.44	VC2							