An Overview of
Analog to Digital and Digital to Analog Converters

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Introduction

A device known as an analog to digital converter (abbreviated A/D) converts an analog voltage signal into a digital number (usually binary) suitable for input to a computer. The inverse function is known as a digital to analog converter (abbreviated (D/A) and converts a digital number (usually binary) from a computer into an analog voltage. The purpose of this note is to briefly describe the internal operation and the characteristics of these devices. These devices are normally purchased as an integrated circuit that is a complete or nearly complete system. Both devices have the same type of specifications so these will be discussed together.

Specifications

Voltage span is the difference between the theoretical **maximum voltage** and the **minimum voltage**. The actual maximum voltage is always one voltage resolution unit below the stated maximum. If the converter is **unipolar** then the minimum voltage is zero. Otherwise, for a **bipolar** device the minimum voltage is negative half the voltage span and the maximum voltage is positive half the voltage span. The maximum actual voltage is always 1 LSB less than the theoretical as indicated by the voltage span. This is necessary so that there is a binary code representing zero in bipolar converters. Although the difference is small, a common error is to assume that the maximum voltage is equal to the theoretical value. Typical voltage spans for common converters are 3, 5, 6, 8.192, 10, and 20 volts.

Maximum voltage = minimum voltage + voltage span – voltage resolution

N is the number of bits or digital lines representing the digital number and typically is between 6 and 16.

Voltage resolution = (voltage span) / 2^N

Conversely, the minimum required number of bits can be determined by solving the above equation for N as shown below. Any fractional part of N is rounded up to the next higher integer.

$$N = \ln(\text{voltage span} / \text{voltage resolution}) / \ln(2)$$

As an example, an 8-bit A/D whose voltage span in 10 volts has a voltage resolution of 39 millivolts. If the a voltage resolution of 1 mV is needed for a 6 volt converter then the required number of bits is 13.

As an example, the maximum output voltage of an 8-bit unipolar D/A whose voltage span is 10 volts is 0 + 10 – 0.039 = 9.961 volts. If the converter were bipolar then the maximum output voltage would be -5 + 10 – 0.039 = 4.961 volts.

Accuracy refers to the accuracy of the voltage span. Typical values are in the 0.5% range.

Linearity refers to the maximum deviation of the output from a theoretically perfect straight line. Inexpensive converters may have linearity errors of several LSBs. Premium converters are often linear to less than one LSB.

Monotonicity refers to whether the output conversion magnitude always increases for an increase in the input magnitude. Most converters are guaranteed to be monotonic over some specified operating conditions. If you operate them outside that range then the output may fail a monotonicity test at some levels. This could be serious in servo systems as monotonic failure is a phase inversion and a limit cycle oscillation becomes possible.

Conversion time is the time required to complete a conversion either from analog to digital or digital to analog. Typical times for common converters are in the tens of microseconds. However, for high-speed converters the time can be in the nanoseconds.

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A/D architectures

Flash method

This is the simplest architecture to understand although it is the most component intensive to implement. The name comes from the fact that the voltage is directly digitized without the use of any algorithm. Thus, the conversion can be extremely fast. A modified version known as pipelined flash significantly reduces the number of components. Figure 1 illustrates a simple 2-bit converter using the flash method.

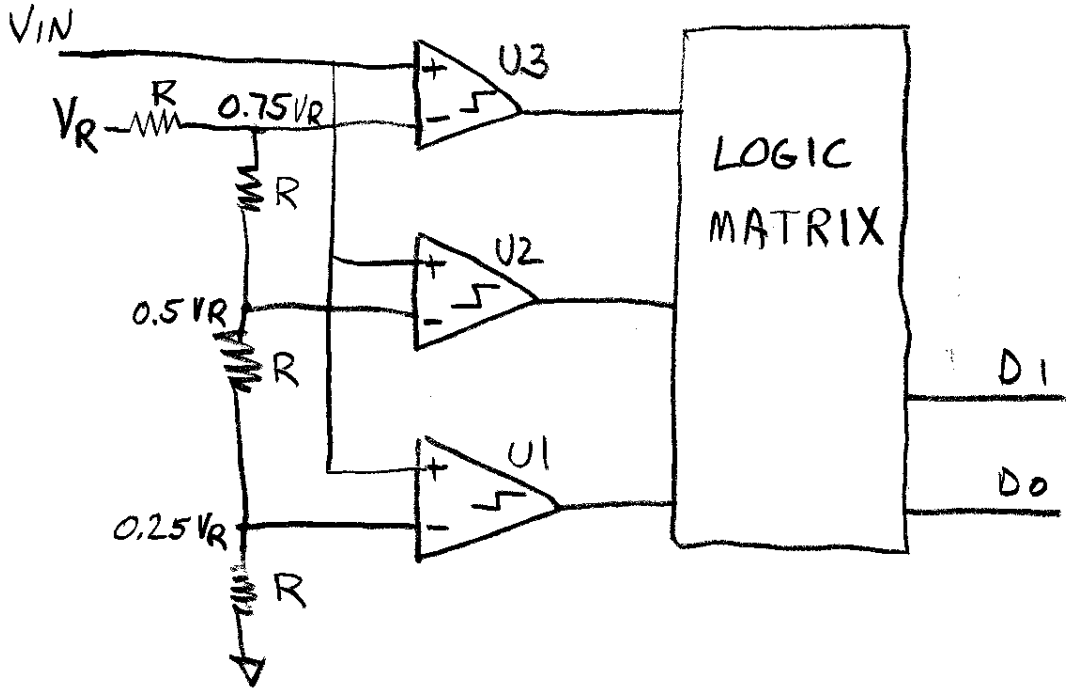

Figure 1: Flash A/D converter

As an example VIN is 2.3 volts and VR is 4.00 volts. Note that VIN is applied to the non-inverting input of all comparators and that a scaled version of VR is applied to each comparator. Comparator, U1, will have a logical '1' output since its reference voltage is 1.00. Comparator, U2, will have a logical '1' output since its reference voltage is 2.00. Comparator, U3, will have a logical '0' output since its reference voltage is 3.00. The logic matrix will map that code into binary 11. The complete truth table for this simple converter is as follows.

U3	U2	U1	Binary output
0	0	0	00
0	0	1	01
0	1	1	10
1	1	1	11

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Successive approximation

This is the most common form of conversion and uses a D/A converter and an algorithm to converge to the digital representation of the analog input voltage. The algorithm begins with all bits to the D/A converter set to 0 except the most significant bit. If the analog input voltage is higher than the D/A output voltage then the D/A bit is latched to a '1'. Then the next least bit of the D/A converter is set to '1' and the resulting output voltage is compared to the input voltage. If the input voltage is higher then this D/A bit is also latched to '1'. This algorithm continues all the way to the least significant bit. It is important for the input voltage to remain stable during the conversion process. Thus, a track-hold (also known as a sample-hold) circuit is often used to briefly "freeze" the analog input. Figure 2 shows the basic structure.

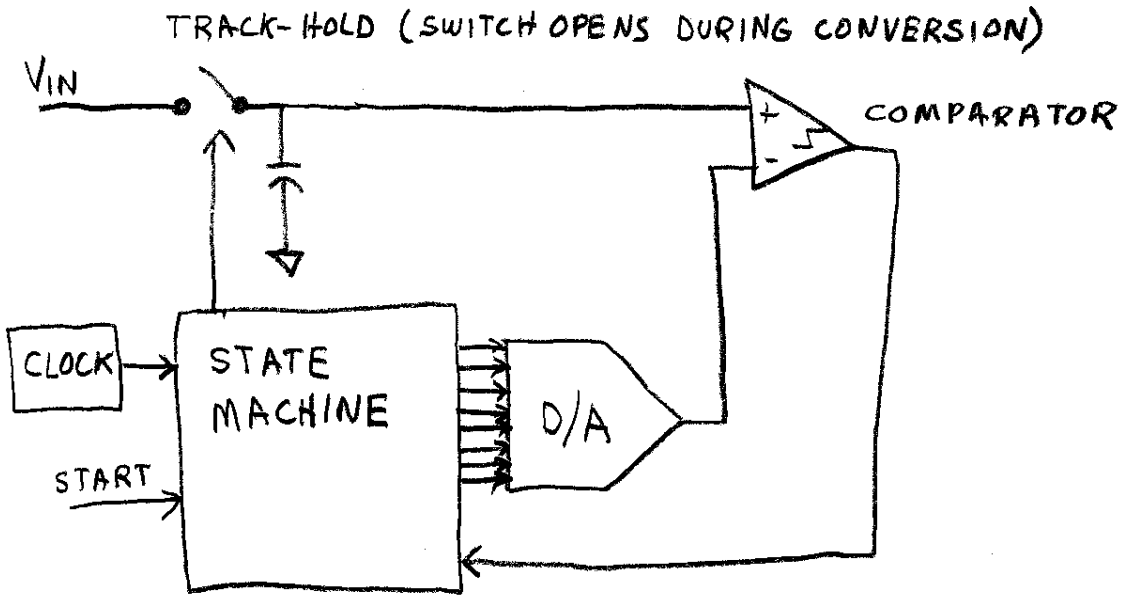

Figure 2: Successive approximation A/D converter

As an example of operation the process of digitizing a 6.9 volt signal will be illustrated using a unipolar 8-bit converter with a maximum voltage of 10.24 (this value is chosen so as to make simple fractional voltages in the example). The conversion process begins with a START signal. The TRACK-HOLD switch then opens so that the signal input to the comparator is constant during the conversion process. The state machine then sets the digital signal to the D/A to binary 10000000 for an output of 5.12 volts. The comparator output is '1' since 6.9 is greater than 5.12. So, the most significant bit is latched. Next, the state machine sets the digital signal to the D/A converter to binary 11000000 for an output of 7.68 volts. The comparator output is '0' since 6.9 is less than 7.68. So, this bit of the D/A number is latched to '0'. The complete process is summarized in the table below.

State Machine Cycle	Binary code	D/A output	Comparator output
1	**1**0000000	5.12 volts	1
2	1**1**000000	7.68	0
3	10**1**00000	6.40	1
4	101**1**0000	7.04	0
5	1010**1**000	6.72	1
6	10101**1**00	6.88	1
7	101011**1**0	6.96	0
8	10101101	6.92	0
9	10101100	Digitized result.	

Dual slope integration

This approach is used in instruments (such a digital voltmeters) and although it is slow (speed is rarely needed in this application anyway) it is simple and capable of high precision and integration is a natural filter that enables good performance in the presence of noise. In operation the input voltage is applied to an analog integrator for a fixed period of time (this is slope 1). Then the time required for an applied reference voltage to cause the integrator to integrate back to zero (this is slope 2) is precisely measured using digital counting methods. This time is a very linear function of the applied voltage and can be highly resolved.

Sigma-delta (also known as Delta-sigma)

This is a new form of A/D that is a 1-bit cousin of the successive approximation method. A complicated form of over-sampling and digital filtering is used to digitize a voltage to many bits of resolution (often 18 to over 24) with perfect linearity. The process can be built on a monolithic integrated circuit and is remarkably inexpensive even though it is by far the most complicated type. The discussion of how this converter works is complicated and the student is referred to application notes on the web sites of companies that manufacture these.

D/A architectures

Switched resistor

This method is shown only as a basis for starting the discussion. Because of the very large resistances required, the method is very impractical for more than a small number of bits of resolution. The electronic switches are typically FETs. This method is, however, the easiest to understand. Figure 3 shows an example of this type of D/A converter.

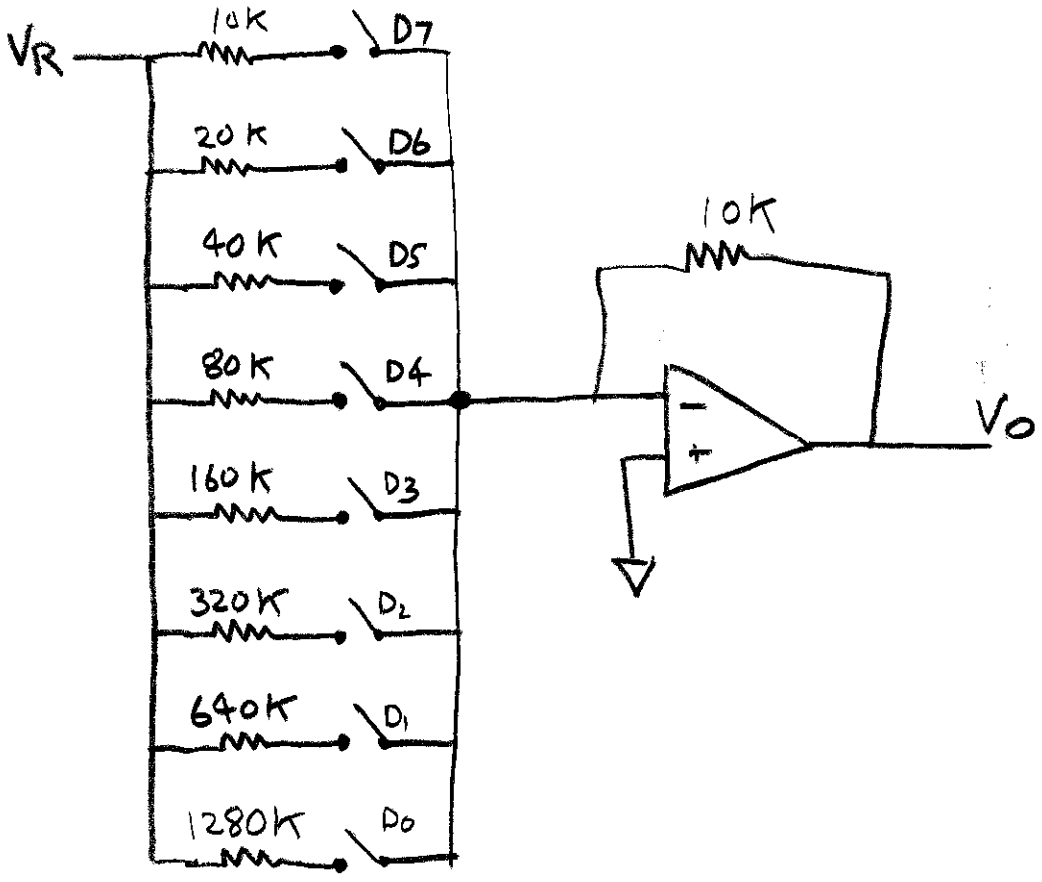

Figure 3: Switched resistor D/A converter

Each of the switches, D0 through D7, are typically constructed using FETs. It is very easy to see the binary weighting of the currents into the summing junction or virtual ground of the op-amp. The output voltage is the sum of these selected currents multiplied by the feedback resistance. This type of circuit is very hard to make using monolithic methods as the resistor values become impractically huge – a 16-bit converter would require a D0 resistor of over 300 megohms! This method has been utilized with discrete components in simple cases requiring only four bits or less.

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R-2R ladder

This method is a special version of the switched resistor method that is very practical to construct on a monolithic integrated circuit. The advantage of this method is that there are only two resistance values no matter how many bits of resolution. Each resistor can be laser trimmed at the factory for high accuracy. The electronic switches are FETs. The practical limit for this method is around 12 bits as accumulative errors lead to non-monotonic behavior. Figure 4 shows an example of this method.

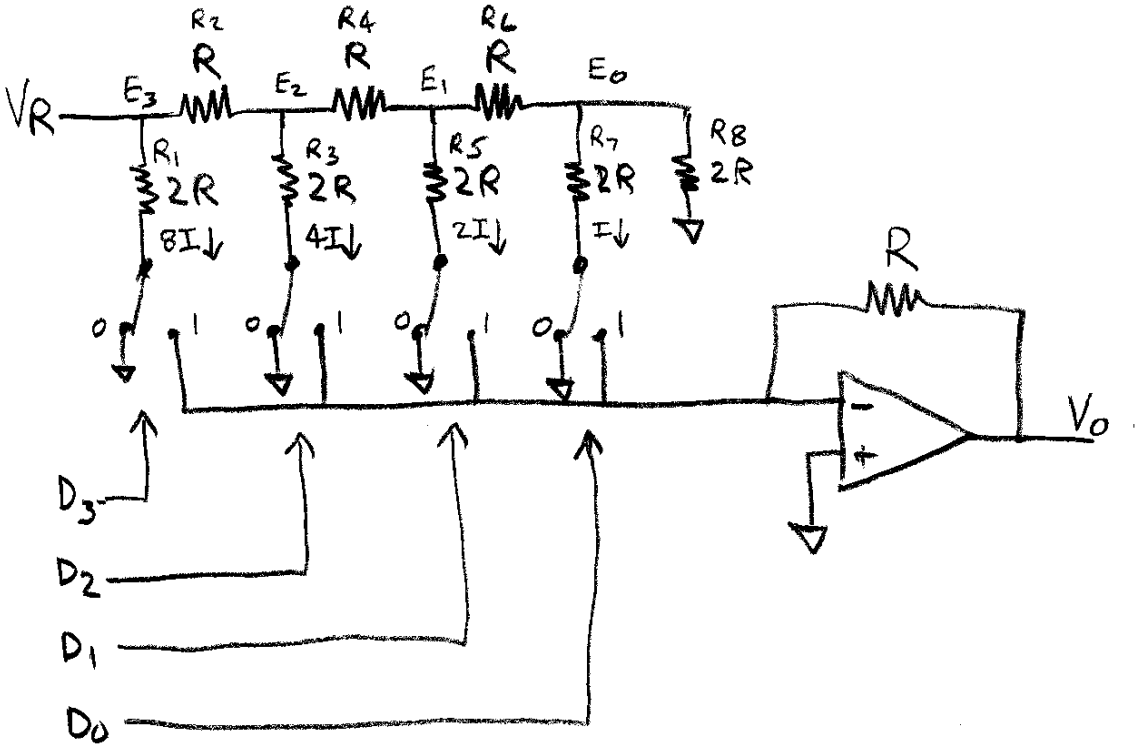

Figure 4: R-2R ladder D/A converter

In operation, an FET switch routes each 2R resistor of the ladder to either ground or the virtual ground of the op-amp. Thus, the current in the resistor is independent of the switch position. This network of resistors creates binary weighted currents. For analysis we start with R7 and R8 which are in parallel for a net resistance of R. The current through R7 is E0/(2R). Because of the voltage divider formed by R6 and R7||R8, it is obvious that E1 is twice E0. Thus, the current through R5 is twice that of R7. It should be noted that R6 + R7||R8 is 2R which when placed in parallel with R5 forms a net resistance of just R. Again, the voltage divider formed by R4 and this resistance means that E2 is twice E1 and the current through R3 is twice that of R5. This process continues for as long as the ladder network is.

The FET switches route the selected currents to the summing junction of the op-amp and the output voltage is the total current multiplied by the feedback resistor.

The advantage of this method is that the resistor values are all closely related and it is easy to integrate this on a monolithic circuit. Laser trimming of the resistors at the manufacturer can result in very precise binary steps of 2 in current.

Switched current source

This method is capable of very high speed although the number of bits is limited for practical reasons to around eight. This method is similar to the switched resistor technique shown previously. Current switching is fundamentally a fast process and is the method of choice for high speed converters operating in the tens of MHz range. Figure 5 shows a simplified example that omits details such as logic levels, etc. Otherwise, the figure would be too complicated. More details are available on manufacturer's web sites.

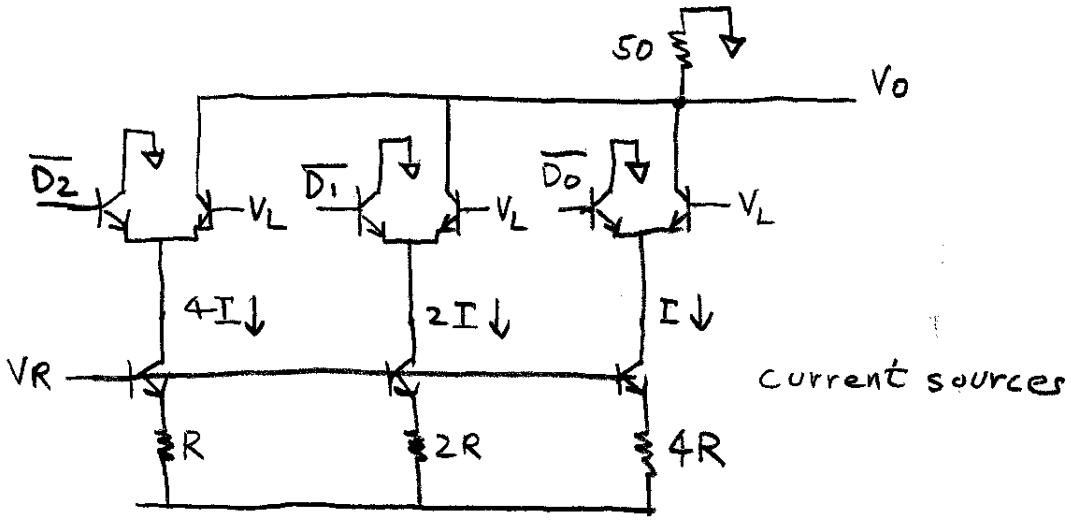

Figure 5: Switched current source D/A converter

In operation, the applied logic level voltages are inverted and translated to be such that a logic low is about 0.9 volts higher than VL – which could be zero or a small negative or positive voltage. An input logic high is translated to be about 0.9 volts below VL. The purpose of this translation is to minimize the required switching voltage at the transistor base in the interest of speed. Thus, either the left transistor of a pair is ON or the right transistor is ON. If the right transistor is ON then the collector current is summed into the output resistor which is often 50 ohms. Op-amps are too slow for this process. The collector currents have a binary weighting so this process directly maps a binary number into an output voltage.

Pulse width modulation (PWM)

This is a 1-bit converter that achieves voltage resolution via time resolution. The output is the average value as determined by the proportion of time the output is high versus low. A low-pass filter smoothes the pulses into the running average. The advantage of this type of converter is that it is absolutely linear and with no non-monotonic issues. It is easy to achieve binary weighted time. It is hard to achieve binary weighted resistors or currents. Figure 6 illustrates the concept.

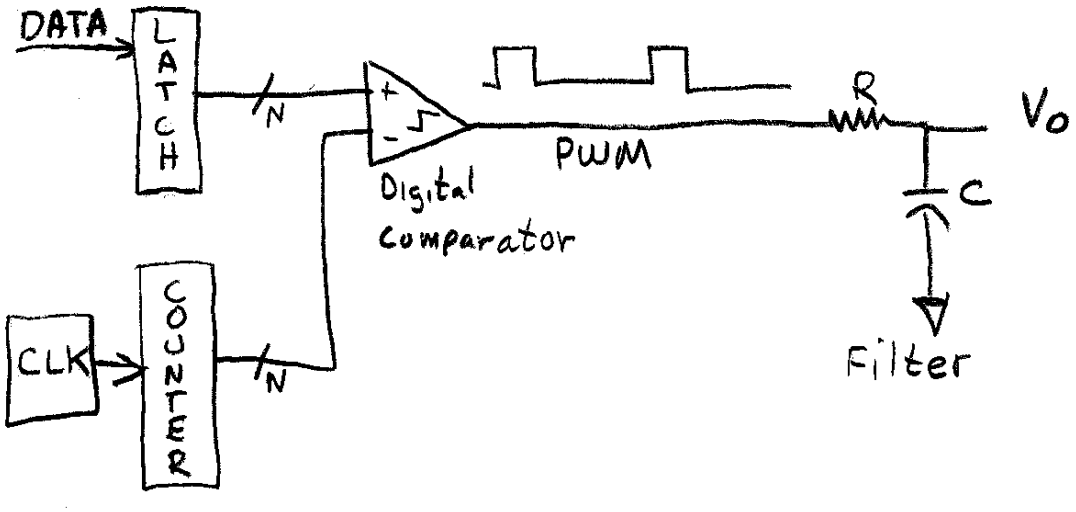

Figure 6: Pulse Width Modulation D/A converter

In operation there is a free-running binary counter with N bits driven by a high frequency oscillator. An N-bit binary number is applied to a digital comparator. The output of the comparator is a logic '1' as long as the data input value is greater than the counter value. The output waveform of the comparator is a logic '1' for exactly the proportion of time that represents the ratio of the applied data value to 2^N. A low-pass filter smoothes this pulse waveform into its DC average.

The update rate for this type of converter is Fo / 2^N. Thus, a 1 kHz update rate for a 12-bit converter would require an oscillator frequency of 4.096 MHz. A 44.1 kHz update rate for a 16-bit converter would require an oscillator frequency of 2.89 GHz – impractically high. However, a complicated but very clever method discussed next can substantially reduce the frequency requirements.

Sigma-delta (also known as Delta-sigma)

This is an extension of the PWM method that can achieve high resolution without the requirement for a high clock frequency. The algorithm uses a complicated form of over-sampling and filtering. This is the most common method of D/A conversion for audio systems. The advantages of this method is that the converter is practically perfectly linear and with no monotonic errors. This method is very complicated but all the

complication is built into a monolithic integrated circuit so the cost is very low. The discussion of how this converter works is complicated and the student is referred to application notes on the web sites of companies that manufacture these.

Homework problems

Note: in most of the following the A/D could be a D/A – it makes no difference to the solution. Answers are in parenthesis.

1. What is the voltage resolution of a 10-bit, 5 volt, unipolar A/D converter? (4.88 mV)

2. What is the voltage resolution of a 12-bit, 20 volt, bipolar A/D converter? (4.88 mV)

3. What is the minimum number of bits of resolution required to achieve 5 mV resolution for an A/D with a voltage span of 6 volts? (11)

4. It is desired to digitize a voltage to a resolution of 2 mV over the range of -7 to +5 volts using a standard A/D with a input range of -10 to +10 volts. What is the minimum number of bits of resolution required? (14)

5. Work through the algorithm, step by step, of how a successive approximation 8-bit A/D converter with a voltage span of 8.192 volts would digitize a 3.39 volt signal. (01101001)