Comparators

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A comparator can be thought of as operational amplifier modified to have a binary output and optimized for speed of response. Like an operational amplifier a comparator has very high gain to the voltage difference between the non-inverting and inverting inputs. However, the output of a comparator is two discrete voltage states (a logical high and low) rather than continuous. The high logical output voltage occurs when the non-inverting input is more positive than the inverting input and a low logical output voltage occurs when the reverse is true. The output of a comparator typically connects to some logic circuit. Comparators serve as the interface between the analog and digital worlds. Comparators are intended to be operated either open-loop or with positive feedback to create a useful hysteresis in its response. Negative feedback is never used. Unlike operational amplifiers the two inputs are almost never equal and will differ by a significant amount. ***At the most fundamental, a comparator is used when a logic level state change is needed in response to an analog signal crossing a threshold voltage.***

The schematic symbols commonly used for comparators are shown in Figure 1. To distinguish a comparator from an operational amplifier a step function or the letter, C, is inserted into the symbol as shown in Figures 1A and 1B. Some other indications have also been used. Unfortunately many modern CAD symbols omit critical details thus causing confusion.

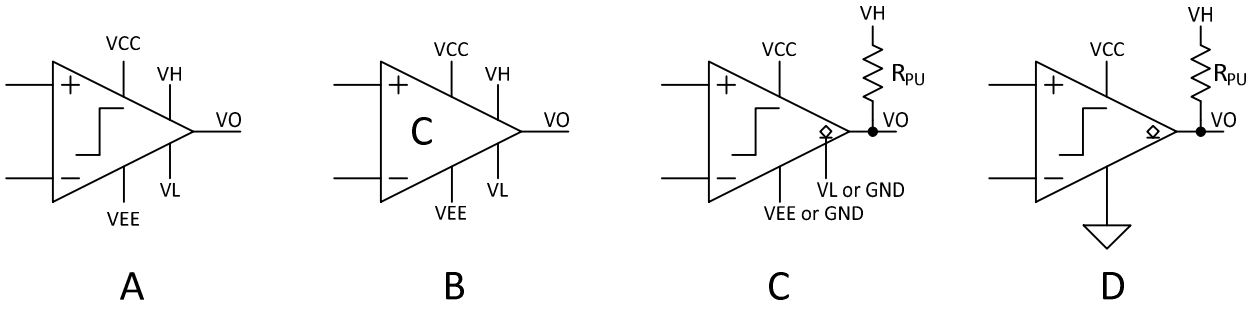

Figure 1: Various comparator symbols

Figures 1A and 1B show the most general version of a comparator. That comparator operates from both positive (V_{CC}) and negative (V_{EE}) power supplies and has separate power connections, V_H and V_L, that are set to match the logic levels of the particular family of digital logic the comparator is being interfaced to. This type of comparator can drive a logic '1' voltage to a load and does not require a pull-up resistor although one might be used.

Many comparators have what is known as open-collector outputs as indicated by the diamond symbol in Figures 1C and 1D. The open-collector output requires an external resistor (known as a pull-up resistor) as shown connected to the desired output logic '1' voltage. The V_L pin is connected to the logic '0' voltage which is often ground but could be some other voltage including negative. The V_{EE} power supply pin is typically a negative voltage but might be ground in some applications.

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The comparator shown in Figure 1D operates on a single positive power supply and has an open-collector output. The lower power supply pin is connected to ground. The output voltage swings between V_H and ground.

Like operational amplifiers, comparators have an input offset voltage typically in the low millivolt range, an input bias current, and an input bias offset current. Just as in operational amplifier circuits the effects of input bias current can be minimized by making the source resistance identical to both the non-inverting and inverting inputs.

Comparators are often used to make a digital signal depending on whether an analog voltage is above or below some threshold. On paper this concept works well but in reality the analog voltage will always have some amount of noise, however small, that will cause the comparator output to switch rapidly back and forth in response to the noise when the analog voltage is within the peak-peak noise voltage of the switching threshold. In some applications this may not be an issue. In other applications the multitude of transitions will cause problems.

The following figures illustrate the noiseless case and a significantly noisy case of a bandwidth limited data reception whose logic '0' output is 2 volts and whose logic '1' output is 4 volts. In Figure 2 the comparator threshold is set to 3 volts and reconstructs the data stream in pure digital form. All works well.

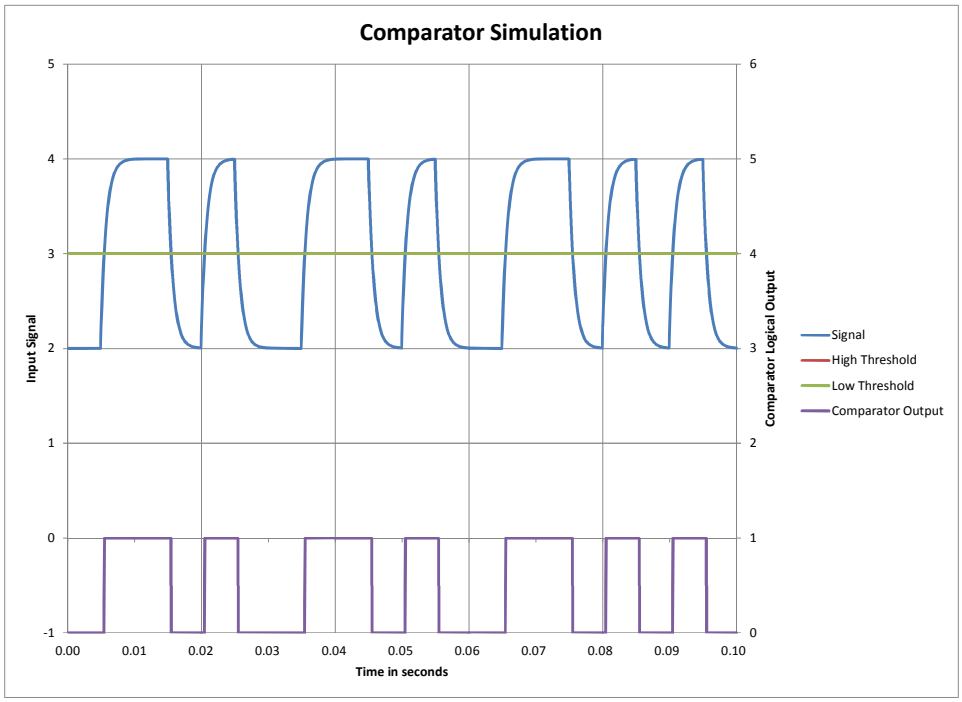

Figure 2: Comparator used to reconstruct a data stream from a bandwidth limited reception

Figure 3 illustrates the case where the reception of the data is corrupted by significant noise. The comparator responds to the noise with a number of extra transitions – usually not desirable.

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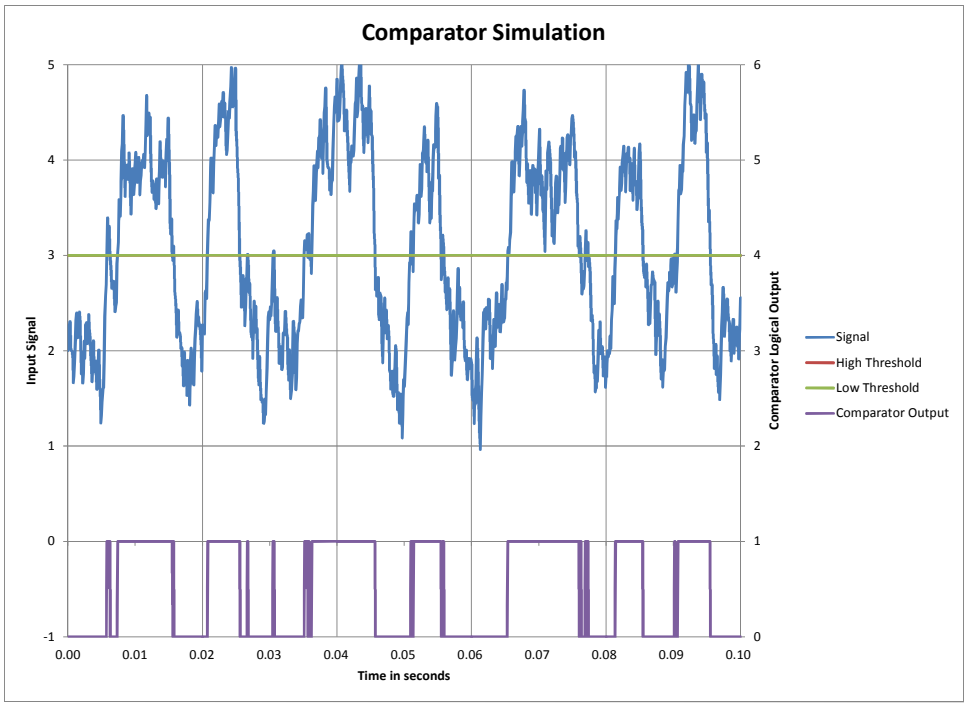

Figure 3: Extra transitions from the comparator in response to a noisy signal

One solution to the noisy situation is to incorporate positive feedback which adds hysteresis to the comparator. That concept is known as a Schmitt Trigger. Once the comparator switches to a logical '1' output then the switching threshold changes so that the comparator won't switch back to a logical '0' until the input signal has dropped below the hysteresis caused by the positive feedback. If the hysteresis band is larger than the peak-peak noise voltage then the comparator will not respond to the noise as demonstrated in Figure 4.

Note the upper and lower thresholds on the plot. Once the signal crosses the upper threshold the comparator output switches to a logical '1' and remains there until the signal falls below the lower threshold where the comparator output switches to a logical '0'. The hysteresis band is larger than the peak-peak noise so no extra transitions occur in the comparator output.

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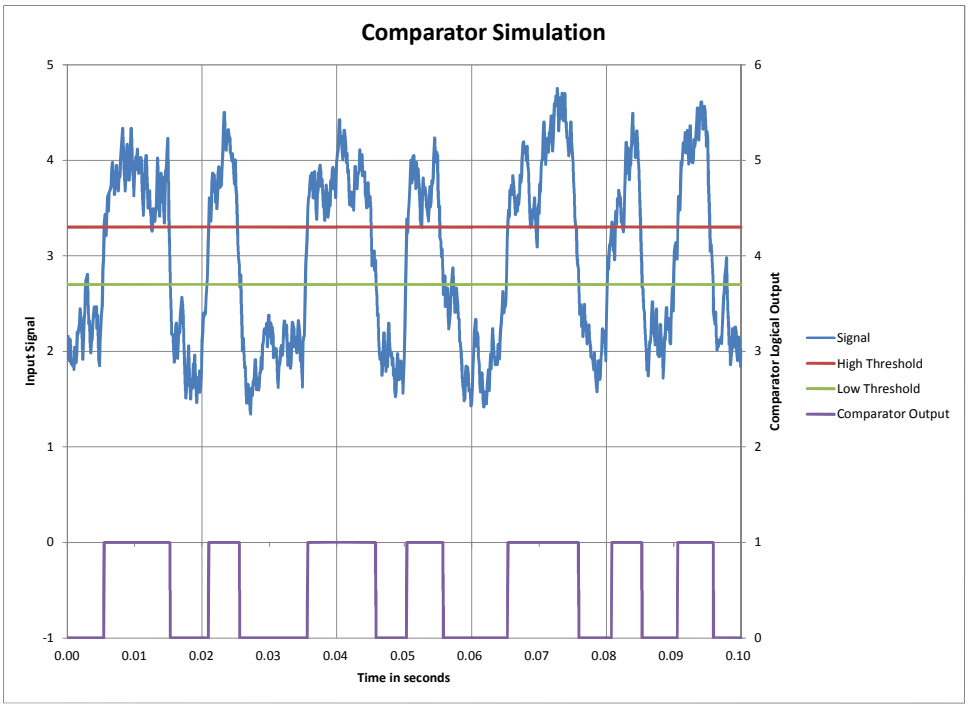

Figure 4: Schmitt Trigger is insensitive to noise

There are two forms of the Schmitt Trigger – the non-inverting form and the inverting form.

The non-inverting form of the Schmitt Trigger is shown in Figure 5. The resistor labeled R_{PU} is a pull-up resistor and is often in the 1,000 to 5,000 ohm range for 5 volt logic and V_H typically connects to +5 volts. The resistor labeled R_F applies positive feedback from the comparator output to the non-inverting terminal resulting in the hysteresis shown in the figure. The hysteresis band is related to the ratio of R_P to R_F.

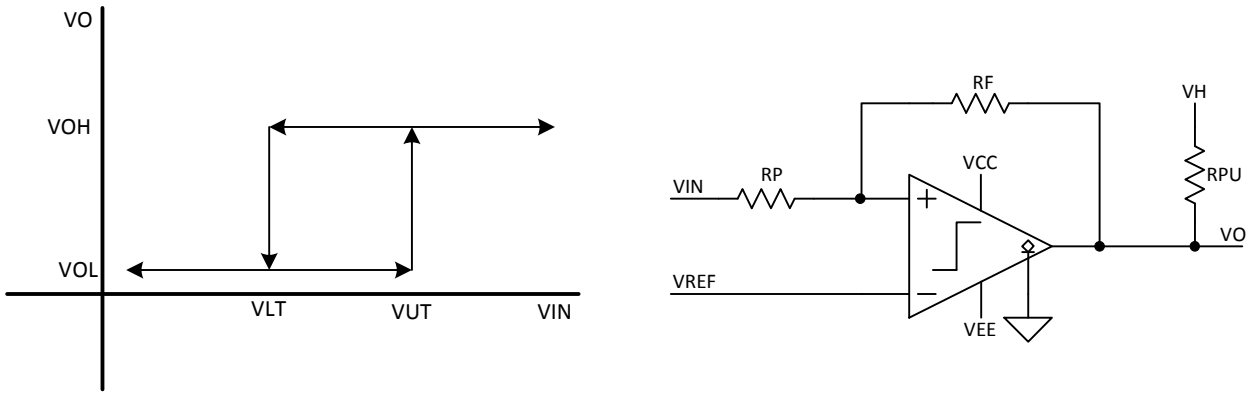

Figure 5: Non-inverting form of Schmitt Trigger

A demonstration of the non-inverting form of the Schmitt Trigger is shown in Figure 6. Observe that the signal at the non-inverting input has a step up and a step down at the Vin- threshold as the output switches thus insuring that the output remains in the new state. Noise is omitted from the figure for clarity.

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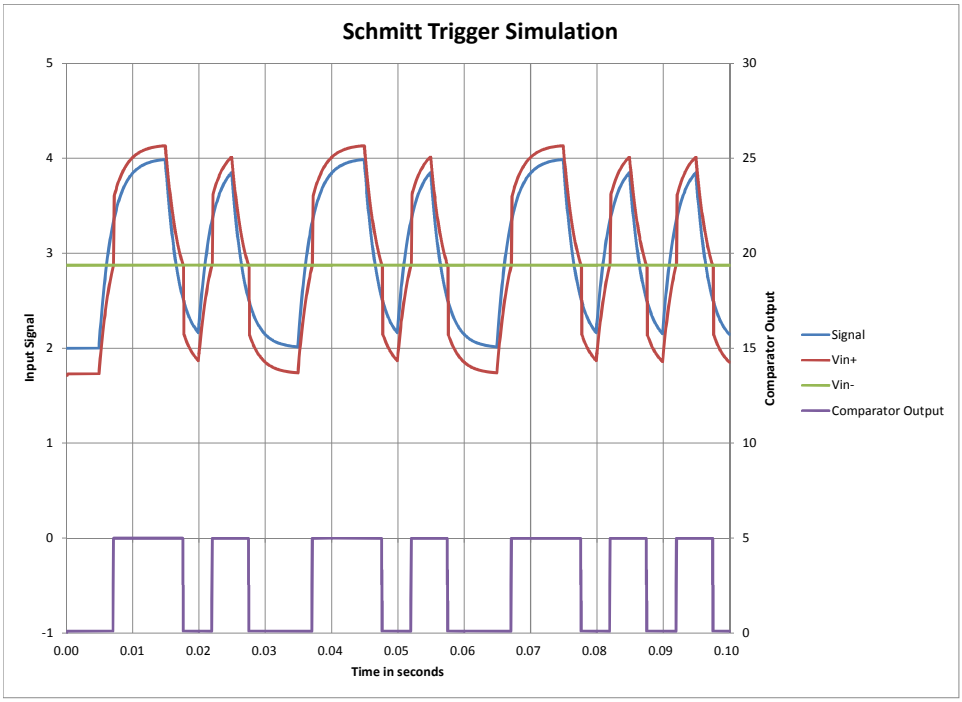

Figure 6: Demonstration of non-inverting form of Schmitt Trigger

The inverting from of the Schmitt Trigger is shown in Figure 7. The only difference is to which terminals the input voltage and reference voltages are applied. Note that the hysteresis diagram is inverted from the previous.

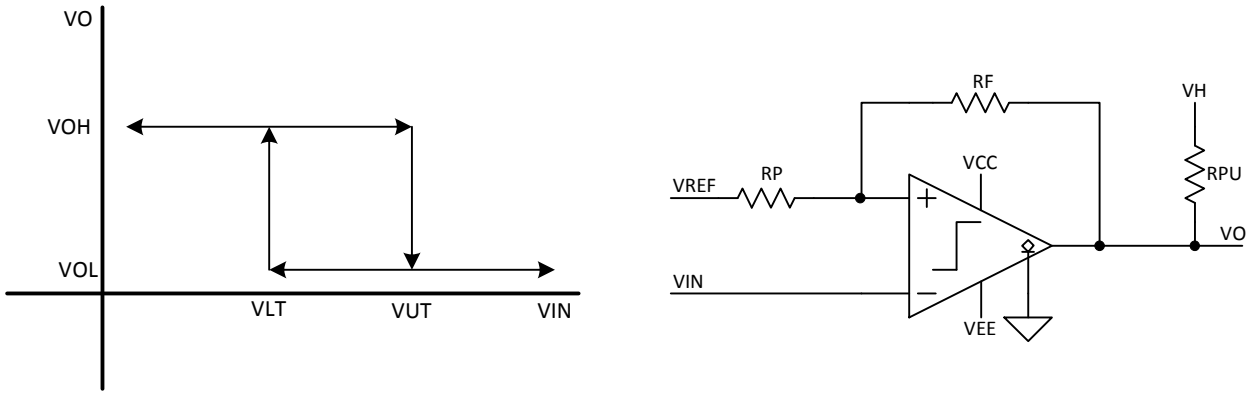

Figure 7: Inverting form of Schmitt Trigger

A demonstration of the inverting form of the Schmitt Trigger is shown in Figure 8. Observe that the signal at the non-inverting input has a step up and a step down at the Vin- threshold as the output switches thus insuring that the output remains in the new state. Observe that the comparator output is phase inverted from the signal input. Noise is omitted from the figure for clarity.

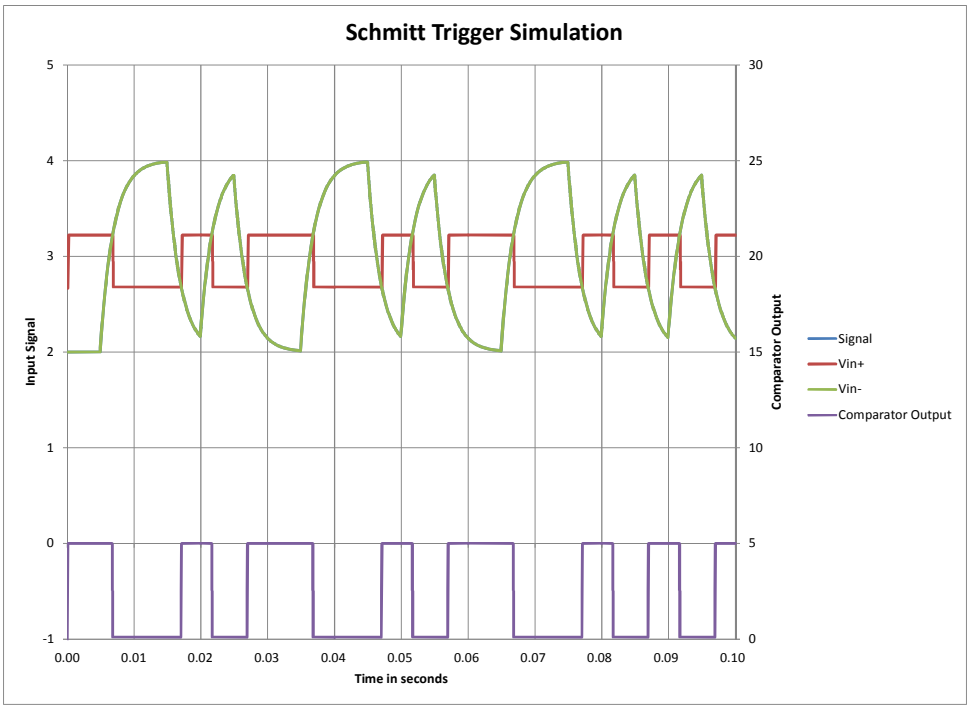

Figure 8: Demonstration of inverting form of Schmitt Trigger

Analysis

Our goal in analysis is to determine the upper threshold voltage, V_{UT}, and lower threshold voltage, V_{LT}, given the reference voltage, V_{REF}, the resistors, R_F and R_P, and the logical '1' output voltage, V_{OH}, and the logical '0' voltage, V_{OL} of the comparator. In a 5 volt system V_{OH} is typically around 5 volts (assuming that R_F is much larger than R_{PU}) and V_{OL} is the collector-emitter saturation voltage of the open collector output transistor – typically in the low 100s millivolt range. A critical point to observe is that when the input voltage is at either threshold that the two inputs of the comparator are exactly the same voltage – the only time that is true. We capitalize on that fact for the analysis.

Non-inverting form derivation

The derivation of the non-inverting form is as follows. We start by assuming that the input voltage is below V_{UT} and that the comparator output voltage is at V_{OL}. Then the voltage at the non-inverting input is found by superposition. We note that when the input voltage is equal to the V_{UT} that the non-inverting input is equal to the inverting input, V_{REF}.

$$V_{REF} = \frac{V_{UT}R_F}{R_P + R_F} + \frac{V_{OL}R_P}{R_P + R_F} \tag{1}$$

We now solve for V_{UT}.

$$V_{UT} = \frac{V_{REF}(R_P + R_F) - V_{OL}R_P}{R_F} \tag{2}$$

The lower threshold voltage is determined similarly.

$$V_{REF} = \frac{V_{LT}R_F}{R_P + R_F} + \frac{V_{OH}R_P}{R_P + R_F} \tag{3}$$

We now can solve for V_{LT}.

$$V_{LT} = \frac{V_{REF}(R_P + R_F) - V_{OH}R_P}{R_F} \tag{4}$$

Inverting form derivation

The derivation of the inverting form is as follows. We start by assuming that the input voltage is below V_{UT} and that the comparator output voltage is at V_{OH}. Then the voltage at the non-inverting input is found by superposition and is the upper threshold voltage.

$$V_{UT} = \frac{V_{OH}R_P}{R_P + R_F} + \frac{V_{REF}R_F}{R_P + R_F} \tag{5}$$

When the input voltage at the inverting input exceeds V_{UT} then the comparator output switches to V_{OL} and because of positive feedback the voltage at the non-inverting input immediately drops thus insuring that the comparator output remains at V_{OL} until the input voltage drops below V_{LT}.

$$V_{LT} = \frac{V_{OL}R_P}{R_P + R_F} + \frac{V_{REF}R_F}{R_P + R_F} \tag{6}$$

Design of Schmitt-trigger

Our job in design is to determine the required resistors, R_P and R_F, and the reference voltage, V_{REF} to achieve given upper and lower threshold voltages, V_{UT} and V_{LT}, based on the comparator output voltages, V_{OH} and V_{OL}. For design we will invert the analytical equations derived earlier. But there is a little problem. There are three unknowns, R_P, R_F, and V_{REF} and we have only two equations. However, if instead of attempting to directly solve for R_P and R_F we instead solve for their ratio then the number of unknowns becomes two and there is a unique solution. We will then conveniently choose one of the resistors and calculate the other using the ratio.

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Non-inverting form design

We start with the analytical equations, 2 and 3, and divide through by R_F to put the resistor values in ratio form. Parentheses are used around the resistor ratios to emphasize that we are only interested in the ratio, not the individual resistors comprising the ratio.

$$V_{UT} = V_{REF}\left(1 + \left(\frac{R_P}{R_F}\right)\right) - V_{OL}\left(\frac{R_P}{R_F}\right) \tag{7}$$

$$V_{LT} = V_{REF}\left(1 + \left(\frac{R_P}{R_F}\right)\right) - V_{OH}\left(\frac{R_P}{R_F}\right) \tag{8}$$

We next subtract Equation 8 from Equation 7.

$$V_{UT} - V_{LT} = (V_{OH} - V_{OL})\left(\frac{R_P}{R_F}\right) \tag{9}$$

We now can solve for the resistor ratio.

$$\left(\frac{R_P}{R_F}\right) = \frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL})} \tag{10}$$

We can substitute the resistor ratio into either Equation 7 or 8 to solve for V_{REF}. We will pick Equation 7 and solve for V_{REF} as shown below.

$$V_{REF} = \frac{V_{UT} + V_{OL}\left(\frac{R_P}{R_F}\right)}{1 + \left(\frac{R_P}{R_F}\right)} \tag{11}$$

We substitute Equation 10 into Equation 11.

$$V_{REF} = \frac{V_{UT} + V_{OL}\left(\frac{V_{UT} - V_{LT}}{V_{OH} - V_{OL}}\right)}{1 + \left(\frac{V_{UT} - V_{LT}}{V_{OH} - V_{OL}}\right)} \tag{12}$$

Equation 12 can be simplified to the following. Applying the equation is simpler than it might first appear since the terms in the parentheses only need to be evaluated once.

$$V_{REF} = \frac{V_{UT}(V_{OH} - V_{OL}) + V_{OL}(V_{UT} - V_{LT})}{(V_{OH} - V_{OL}) + (V_{UT} - V_{LT})} \tag{13}$$

Example 1: Design a non-inverting Schmitt Trigger to switch on threshold voltages of V_{UT} = 3.3 volts and V_{LT} = 2.7 volts. V_{OH} is 5 volts and V_{OL} is 0.1 volts. Using Equation 10, (R_P/R_F) = 0.167. We chose R_P = 10K so R_F calculates to be 60K. Using Equation 13 V_{REF} = 2.872 volts. Figure 9 is a simulation of this design. Observe that the voltage at Vin+ jumps up or down by 0.6 volts at the transition.

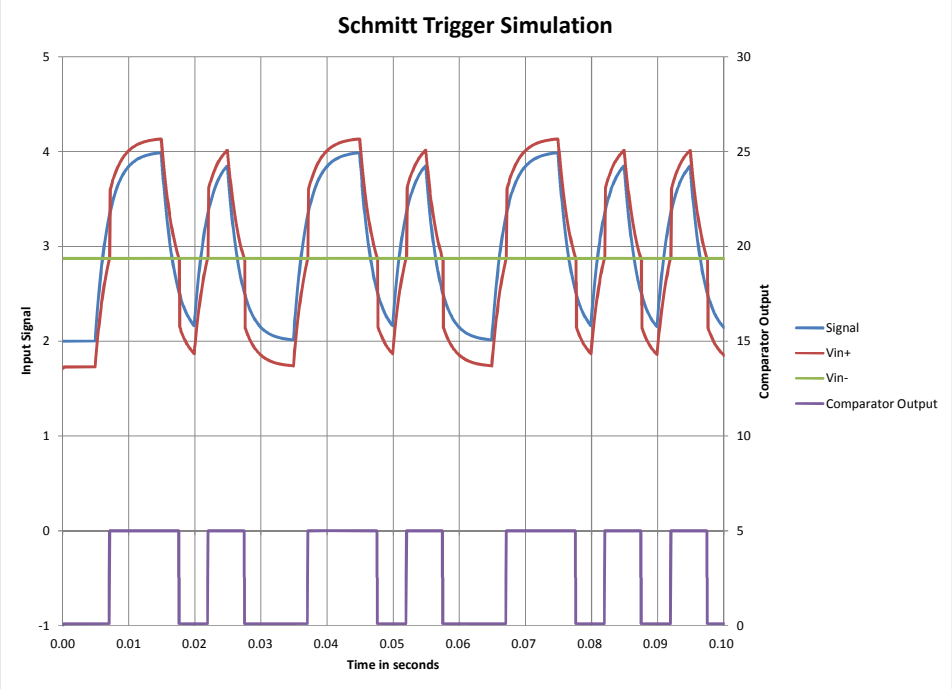

Figure 9: Simulation of design

Inverting form design

We start with the analytical equations, 5 and 6, and divide through by R_F to put the resistor values in ratio form. Parentheses are used around the resistor ratios to emphasize that we are only interested in the ratio, not the individual resistors comprising the ratio.

$$V_{UT} = \frac{V_{OH}\left(\frac{R_P}{R_F}\right)}{1 + \left(\frac{R_P}{R_F}\right)} + \frac{V_{REF}}{1 + \left(\frac{R_P}{R_F}\right)} \tag{14}$$

$$V_{LT} = \frac{V_{OL}\left(\frac{R_P}{R_F}\right)}{1+\left(\frac{R_P}{R_F}\right)} + \frac{V_{REF}}{1+\left(\frac{R_P}{R_F}\right)} \tag{15}$$

We subtract Equation 15 from Equation 14 so that the V_{REF} terms vanish.

$$V_{UT} - V_{LT} = (V_{OH} - V_{OL})\left(\frac{\left(\frac{R_P}{R_F}\right)}{1+\left(\frac{R_P}{R_F}\right)}\right) \tag{16}$$

The only unknown is the resistor ratio which we can now solve for.

$$\frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL})}\left(1+\left(\frac{R_P}{R_F}\right)\right) = \left(\frac{R_P}{R_F}\right) \tag{17}$$

We factor (R_P/R_F) and locate on one side of the equation.

$$\left(\frac{R_P}{R_F}\right)\left(\frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL})} - 1\right) = -\frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL})} \tag{18}$$

We can now obtain the rough solution for (R_P/R_F).

$$\left(\frac{R_P}{R_F}\right) = \frac{\frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL})}}{1 - \frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL})}} \tag{19}$$

After some simplification we have the final solution for (R_P/R_F).

$$\left(\frac{R_P}{R_F}\right) = \frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL}) - (V_{UT} - V_{LT})} \tag{20}$$

We can substitute the resistor ratio into either Equation 14 or Equation 15 to calculate V_{REF}. We will choose Equation 14.

$$V_{REF} = V_{UT}\left(1+\left(\frac{R_P}{R_F}\right)\right) - V_{OH}\left(\frac{R_P}{R_F}\right) \tag{21}$$

We now substitute the solution for (R_P/R_F) which initially makes a complicated looking equation.

$$V_{REF} = \left(1 + \frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL}) - (V_{UT} - V_{LT})}\right) - V_{OH}\left(\frac{(V_{UT} - V_{LT})}{(V_{OH} - V_{OL}) - (V_{UT} - V_{LT})}\right) \quad (22)$$

However, Equation 22 simplifies to the following. The terms in the parentheses are repeated so we only have to evaluate them once.

$$V_{REF} = \frac{V_{UT}(V_{OH} - V_{OL}) - V_{OH}(V_{UT} - V_{LT})}{(V_{OH} - V_{OL}) - (V_{UT} - V_{LT})} \quad (23)$$

Example 2: Design an inverting Schmitt Trigger to switch on threshold voltages of V_{UT} = 3.3 volts and V_{LT} = 2.7 volts. V_{OH} is 5 volts and V_{OL} is 0.1 volts. Using Equation 20, (R_P/R_F) = 0.140. We chose R_P = 10K so R_F calculates to be 71.4 K. Using Equation 23 V_{REF} = 3.063 volts.

Two-comparator Schmitt Trigger

An alternate circuit for implementing a Schmitt Trigger using a pair of comparators is shown in Figure 10. This circuit has the advantage that the upper and lower thresholds are set by specific voltages rather than by a complicated interaction of the comparator output signal swing and the various resistors. This circuit is capable of high precision in the thresholds.

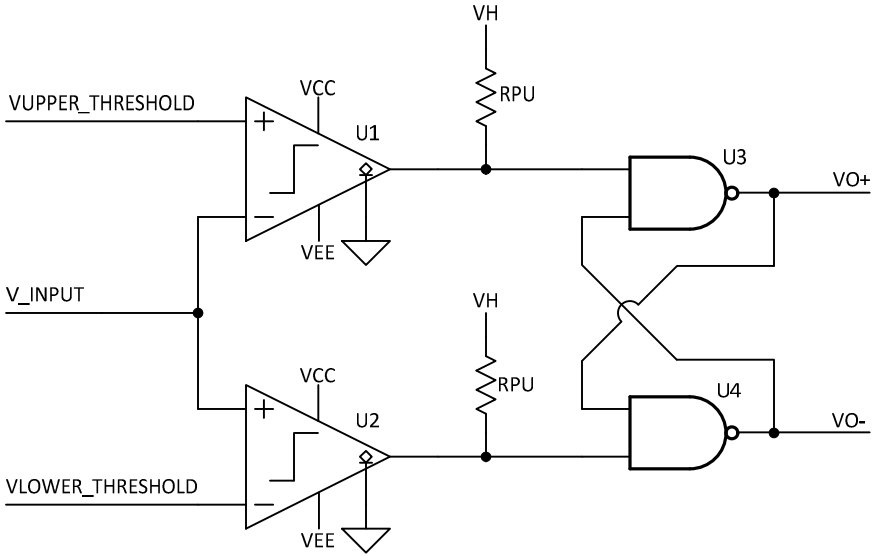

Figure _: Two comparator form of Schmitt Trigger

The moment the input voltage exceeds the upper threshold the output of comparator, U_1, goes to a logical '0' and the output of NAND gate, U_3, goes to a logical '1' and latches at that level

because of the RS flip-flop formed by the connections of U_3 and U_4. Any noise on the input voltage that will cause U_1 to switch will have no effect on the output of U_3.

The moment the input voltage drops below the lower threshold the output of comparator, U_2, goes to a logical '0' and the output of NAND gate, U_4 goes to a logical '1' and latches at that level because of the RS flip-flop formed the connections of U_3 and U_4. Any noise on the input voltage that will cause U_2 to switch will have no effect on the output of U_4.

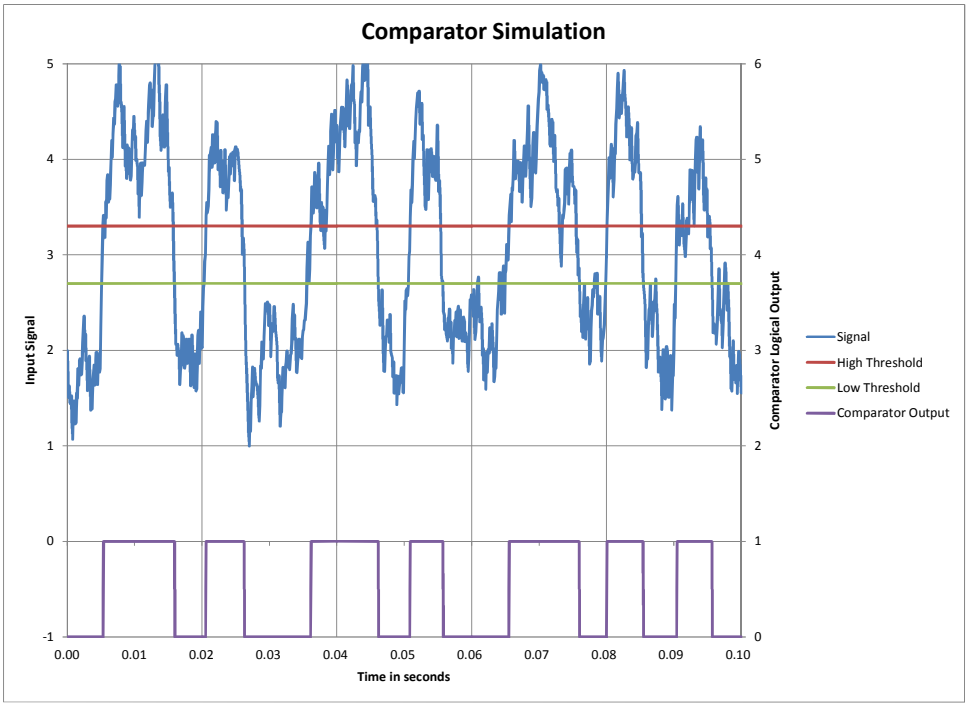

Figure 10: Hysteresis using dual thresholds makes circuit insensitive to noise

Comparator applications

Window comparator

A window comparator circuit produces a logical true output only when the input signal is between an upper and lower threshold. One application of a window comparator is shown in Figure 11. The circuit lights the blue LED if the input voltage is below the low threshold, the green LED if the input voltage is between the two thresholds – i.e. the true window function, and the red LED if the input voltage is above the high threshold. This circuit is only useful for driving low currents (less than about 5 mA) to the LEDs. Resistors, R_1, R_2, and R_3 are used to set the LED currents so that all LEDs have about the same brightness to the human eye. Note that diodes, D_2 and D_3 form an AND gate so that the green LED only lights when V_{IN} is between the two thresholds. Observe that U_1 has to sink the sum of the current through the red LED and

also through R_2 – not the preferred situation but a compromise for the circuit to be simple for introduction to students.

Challenge: Can an enterprising student figure out some clever modification to the circuit that solves that issue while retaining the simplicity? Hint: Think outside the proverbial box and don't become locked into certain aspects of the circuit as you see them. Good design engineers master that concept. No guarantees that such a modification is possible – or not possible.

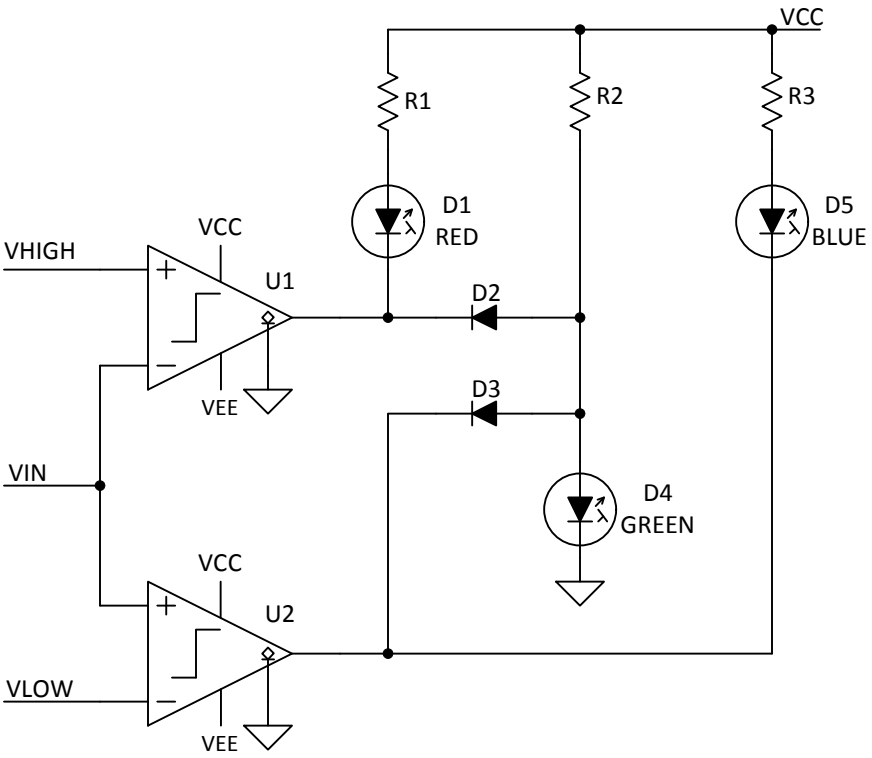

Figure 11: Simple window comparator

Figure 12 shows a version of the previous window comparator that is not limited to the current sinking ability of the comparators. The circuit can drive higher currents through the LEDs since transistors, Q_1, Q_2, and Q_3 serve as current buffers. Resistors R_1, R_7, and R_2, R_8 are calculated so that the transistors go into definite voltage saturation at the lowest beta they might have. R_4 is of such value so that at the minimum possible beta of Q_2 that the required base current only causes a few tenths of a volt (perhaps around 0.5) drop across R_4.

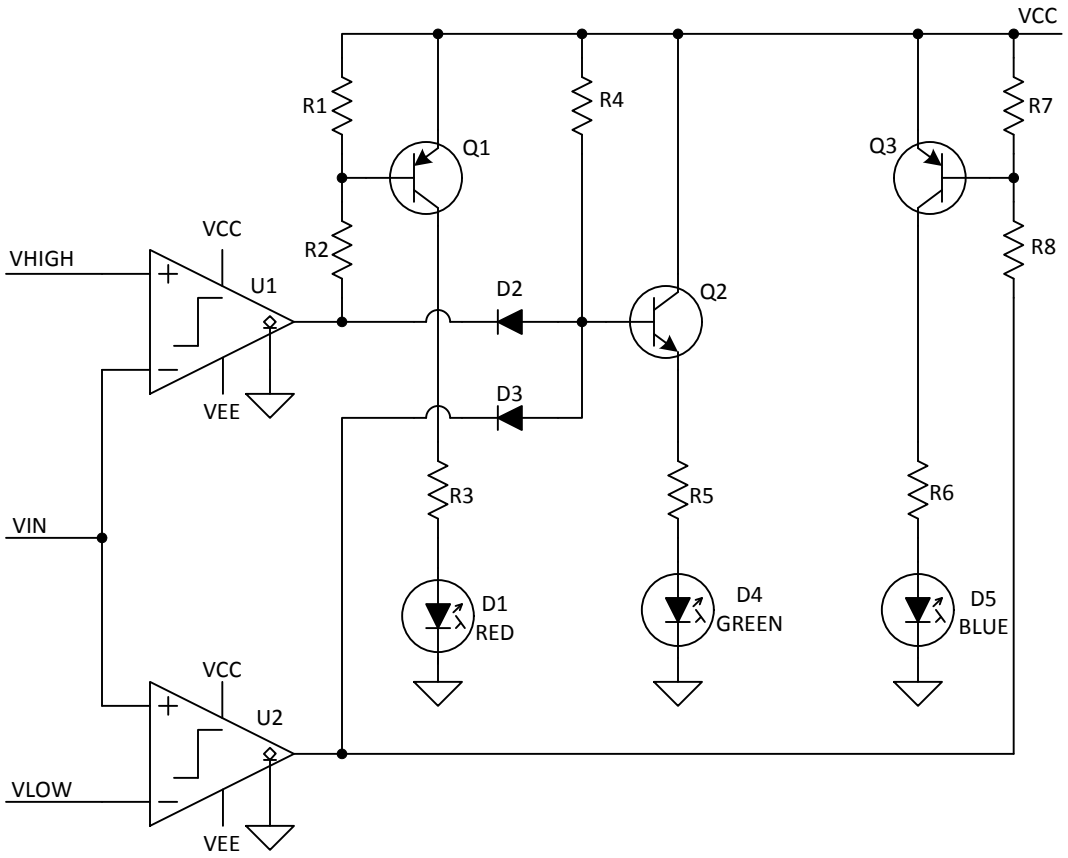

Figure 12: Window comparator with high-current LED drive

State machine oscillator

Figure 13 illustrates the two-comparator Schmitt Trigger used to build an oscillator that produces a square wave and a triangle wave. The purpose of R_4 is to make the output of U_4 go all the way to +5 volts for a logical '1'. That resistor is typically around 1,000 ohms. When the output of U_4 is a logical '0' the integrator formed by R_5, C_1, and U_1 integrates upwards towards the high threshold of 2.5 volts. When that threshold is reached, comparator U_2 goes low thus causing U_4 to go high and in turn the output of U_5 to go high. The integrator now integrates towards the low threshold. When the low threshold is reached the output of comparator, U_3, goes low thus causing U_5 to go high and in turn causing the output of U_4 to go low and the oscillation cycle repeats indefinitely.

A small threshold voltage of 0.05 volts is shown for comparator, U_3. This is to compensate for the fact that U_1 may not go all the way to ground and that comparator, U_3 might have an input offset of such polarity to be unfavorable to the true low threshold to be reached. Depending on the specifications of the actual parts used this small non-zero threshold can probably be significantly reduced – but it can never be truly zero for the circuit to always work for any parts.

Comparators

Just because a prototype circuit might happen to work when the margins are very small does not mean that production circuits will all work.

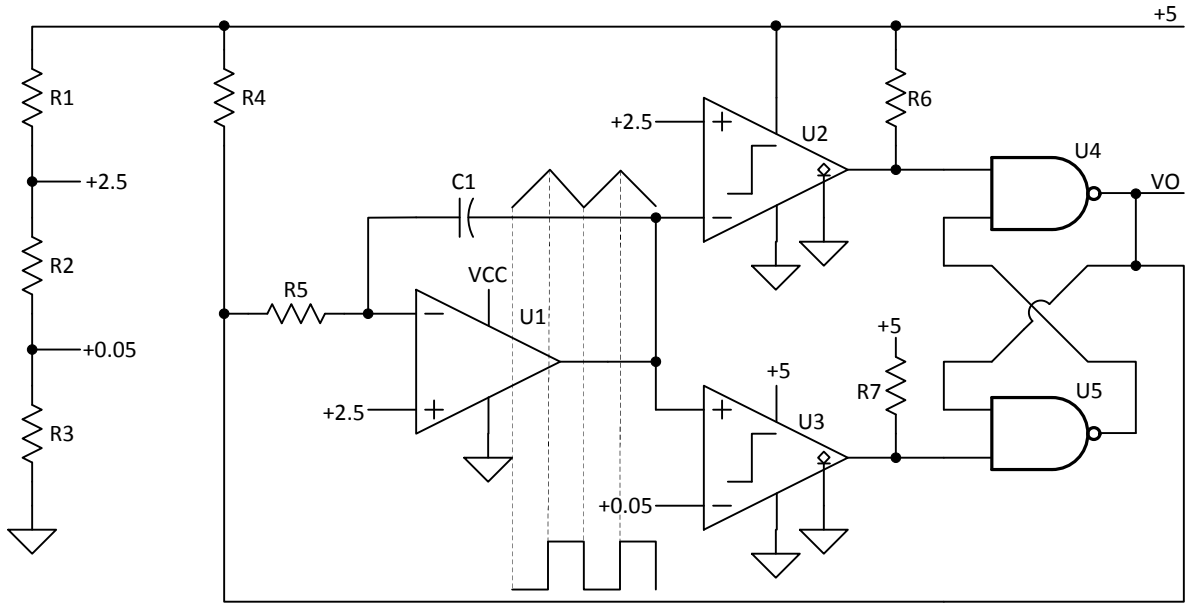

Figure 13: Illustration of state-machine oscillator using comparators

A good example of a state-machine oscillator is the LM555 timer I.C. It is based on a very similar concept to the circuit in Figure 13.

Pulse Width Modulator

A rudimentary pulse-width modulator based on the state-machine oscillator in Figure 13 is shown in Figure 14. A single comparator Schmitt Trigger is used to replace the cross coupled NAND gates in the state-machine oscillator. R_{12} is used to pull the output of comparator, U_4 up to 5 volts when its output is a logical '1'. Resistors R_7 through R_{10} are typically all the same value – often 10K. Resistors, R_7 and R_8, form a voltage divider such that the open-circuit output voltage is 2.5 volts when the output of comparator, U_3, is a logical '1'. The same applies to resistors, R_9 and R_{10}, in relation to the output of comparator, U_2. Positive feedback resistor, R_{11}, causes the voltage at the non-inverting input of comparator, U_4, to be about 3.3 volts when the comparator output is a logical '1' and about 1.7 volts when the comparator output is a logical '0'. When the output of comparator, U_4, is a logical '0' the integrator formed by R_5, C_1, and U_1 integrates upwards towards the high threshold. When the high threshold is reached, the output of comparator, U_2, goes low causing the output of comparator, U_4, to latch to a high state (~5V). The integrator then slews downwards towards the low threshold (0.05V). When that low threshold is reached the output of comparator, U_3, goes low thus causing the output of comparator, U_4 to latch to a zero state and the oscillation cycle continues indefinitely.

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The voltage divider formed by resistors, R_5 and R_6, scales the triangle waveform at the output of U_1 to vary between ~0 and 1 volt – for this example – other voltage ranges could be used. The range of V_{IN} for full control of the output duty cycle over the range of 0 to 100% is 0 to 1 volts. When the scaled triangle waveform is lower than V_{IN} then the output of comparator, U_5, is a logical '1'. When V_{IN} is small then the logical '1' time is brief. If V_{IN} is 1 volt or greater then the output of U_5 is always a logical '1'.

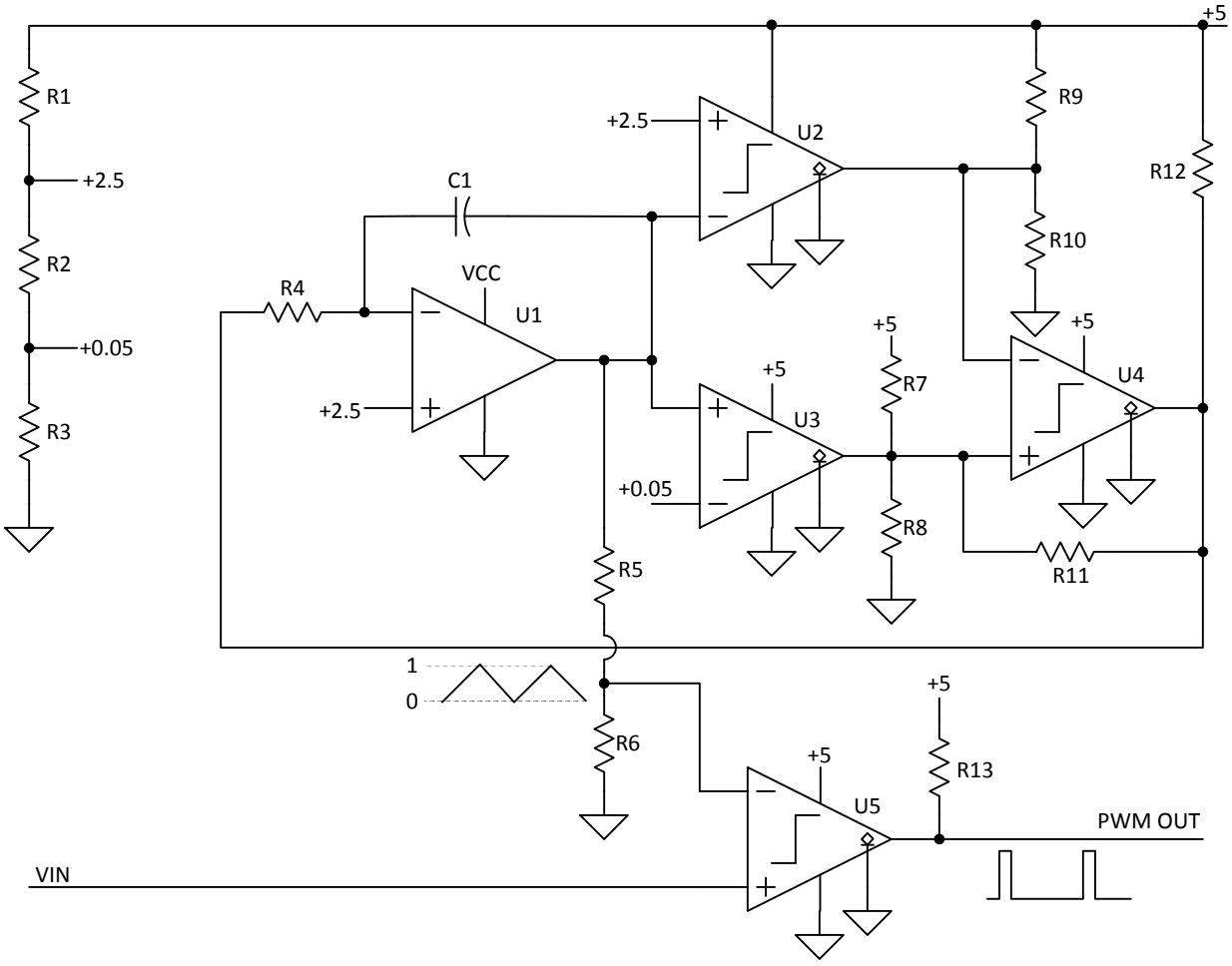

Figure 14: Demonstration of voltage pulse width modulation