State Machine Oscillators

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Introduction

State machine oscillators are based on periodic charging and discharging a capacitor to specific voltages using one or more voltage comparators and usually an RS flip-flop. These are non-linear oscillators so s-plane methods are not applicable.

Simple comparator oscillator

The circuit shown in Figure 1 is a simple state machine oscillator using a Schmitt trigger with an RC time constant in the negative feedback path. Being simple it is lacking some features such as temperature stability and load independence but if those are not important then this oscillator can be useful. The capacitor charges and discharges nearly symmetrically between the upper and lower Schmitt thresholds. The output of the comparator is close to a square wave. R_{PU} is a pull-up resistor generally around 4.7K and is required for most comparators since outputs are usually open-collector. The pair of R_B resistors creates a voltage equal to half the power supply with a source resistance of $R_B/2$. The hysteresis band (Schmitt threshold voltages) is determined by this value and R_F.

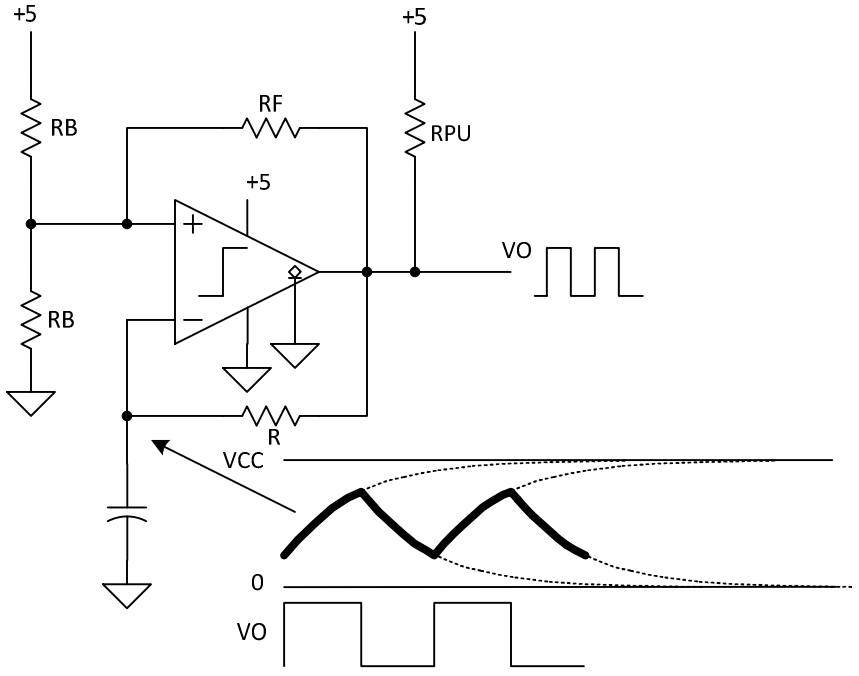

Figure 1: Simple Schmitt trigger oscillator

Analysis is as follows. The combination of the two R_B resistors and R_F resistor forms a hysteresis band symmetrical about 2.5 volts. Those switching levels can be calculated

using the equations in the notes for Schmitt triggers. We will assume an upper threshold, V_{UT}, of 3 volts and a lower threshold, V_{LT}, of 2 volts. The charging of the capacitor from V_{LT} to V_{UT} is described by the following equation.

$$V_{C(t)} = V_{LT} + (V_{CC} - V_{LT})\left(1 - e^{(-t/RC)}\right) \tag{1}$$

We are interested in the charging time, t_C, it takes to reach V_{UT}.

$$V_{UT} = V_{LT} + (V_{CC} - V_{LT})\left(1 - e^{(-t_C/RC)}\right) \tag{2}$$

Solving for t_C gives

$$t_C = RC \ln\left[\frac{V_{CC} - V_{LT}}{V_{CC} - V_{UT}}\right] \tag{3}$$

The discharging of the capacitor from V_{UT} to V_{LT} is described by the following equation.

$$V_{C(t)} = V_{UT} e^{(-t/RC)} \tag{4}$$

We are interested in the discharge time, t_D, it takes to reach V_{LT}.

$$V_{LT} = V_{UT} e^{(-t_D/RC)} \tag{5}$$

Solving for t_D gives

$$t_D = RC \ln\left[\frac{V_{UT}}{V_{LT}}\right] \tag{6}$$

The frequency of oscillation is calculated as follows.

$$F = \frac{1}{t_C + t_D} = \frac{1}{RC \ln\left[\frac{V_{CC} - V_{LT}}{V_{CC} - V_{UT}}\right] + RC \ln\left[\frac{V_{UT}}{V_{LT}}\right]} \tag{7}$$

The final result is

$$\boxed{\boldsymbol{F = \frac{1}{RC\left[\ln\left[\frac{V_{CC} - V_{LT}}{V_{CC} - V_{UT}}\right] + \ln\left[\frac{V_{UT}}{V_{LT}}\right]\right]}}} \tag{8}$$

State Machine Oscillators

Advanced comparator oscillator

The circuit shown in Figure 2 uses two comparators for more precise switching points than can be achieved in the previous simpler circuit. With some refinements, this circuit is capable of very good stability and a variety of versions are used. As shown the output will be a square wave with a common charge/discharge path. If V_{UT} and V_{LT} are non-symmetrical about half the power supply voltage then a rectangular output waveform with a duty cycle higher or lower than 0.5 is produced. This circuit has the advantage that the threshold voltages, V_{UT} and V_{LT}, are applied to the circuit rather than being derived as a function of other circuit parameters. This makes the circuit much more predictable in its operation. When the output is low, the lower NAND gate is high and the capacitor charges upwards. When the upper threshold, V_{UT}, is reached the upper comparator switches low which changes the state of the RS flip-flop so that the output is now high. The lower NAND gate is now low and discharges the capacitor towards zero. When the lower threshold, V_{LT}, is reached the lower comparator switches low which changes the state of the RS flip-flop so that the output is high again and the process repeats. The math for this circuit is identical to the math of the previous circuit.

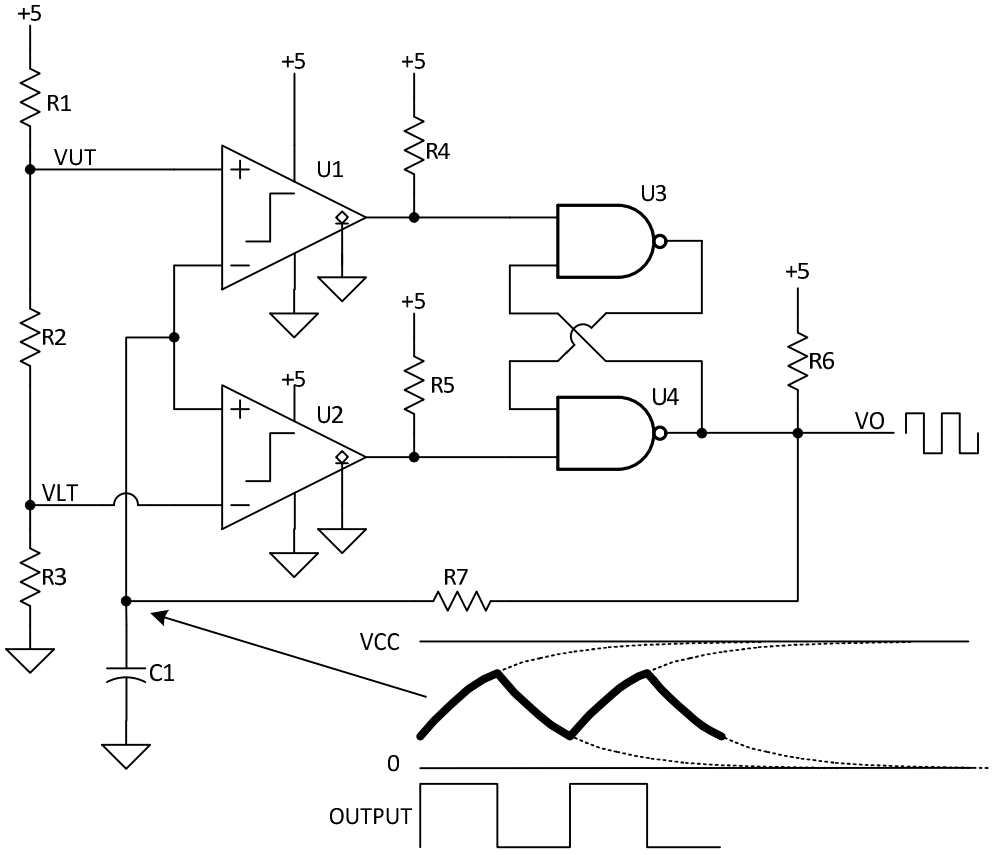

Figure 2: Advanced comparator oscillator

State Machine Oscillators

LM555 Timer

The LM555 timer is a general purpose version of the advanced comparator oscillator in monolithic chip form that can implement a variety of timing and oscillator functions using an external capacitor and one or more resistors. Its block diagram along with the typical external circuit is shown in Figure 3. Observe that it has two comparators with fixed upper and lower thresholds equal to 2/3 and 1/3 of V_{CC} respectively. This makes many timing functions independent of the actual power supply voltage. The outputs of the comparators go to an RS flip-flop. Negative going output of the comparators causes the RS flip-flop to change state. A reset pin which is normally connected to V_{CC} can force the output low if brought to ground potential. The FM pin (normally either left open or connected to a bypass capacitor to ground for better overall stability) can be used to dynamically change the switching thresholds for frequency modulation effects. The discharge pin is used to discharge the timing capacitor.

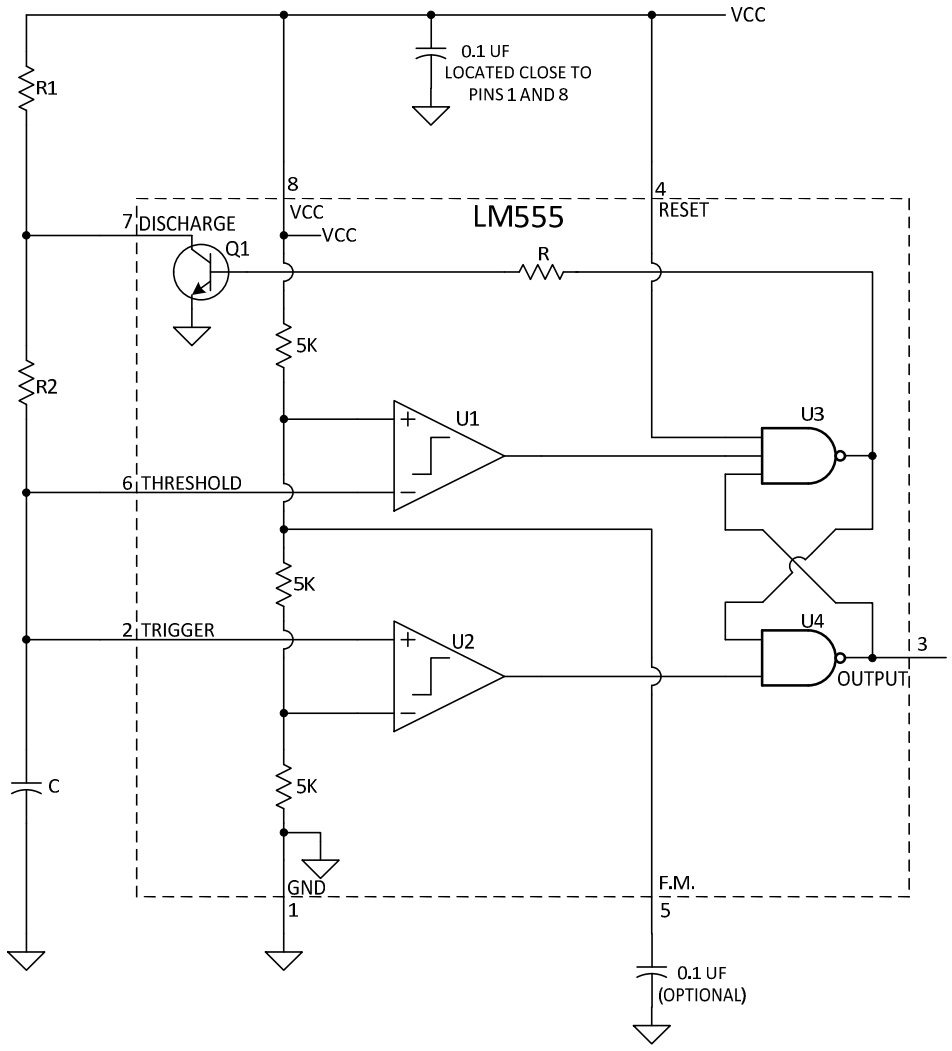

Figure 3: LM555 block diagram and external circuit

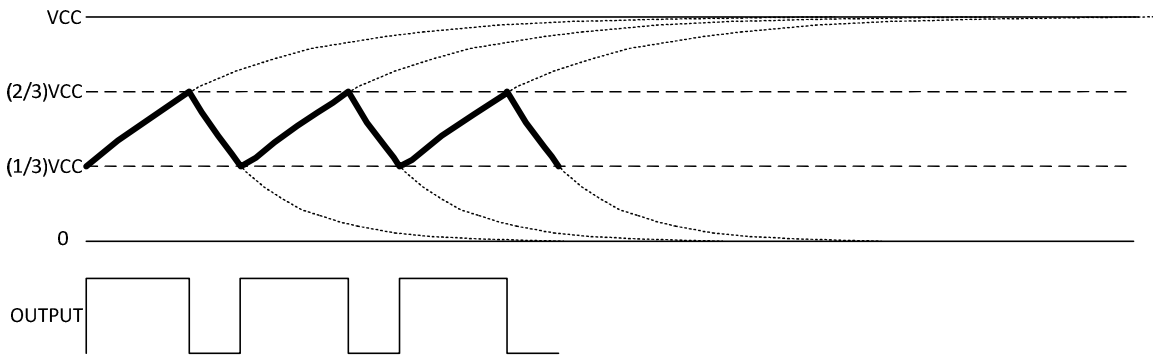

Figure 4: Waveforms of LM555 timer

Operation is as follows. When the output (pin 3) is low, the discharge pin (pin 7) is open and the capacitor charges towards V_{CC} through R_1 plus R_2. When the voltage on the capacitor reaches the upper threshold (2/3 V_{CC}) the output switches to low and the discharge pin switches to ground thus discharging the capacitor through R_2. When the voltage on the capacitor falls to the lower threshold (1/3 V_{CC}) the output switches to high and the process repeats. The timing cycle is broken into two regions, charging and discharging. Each of these has a separate equation.

For the charging region the capacitor is charged towards V_{CC} through the series combination of R_1 and R_2. The general charging equation is as follows.

$$V_{C(t)} = \left(\frac{1}{3}\right)V_{CC} + \left(V_{CC} - \left(\frac{1}{3}\right)V_{CC}\right)\left(1 - e^{-\frac{t}{\tau}}\right) \tag{9}$$

We are interested in the time, t_1, it takes to charge from (1/3)V_{CC} to (2/3)V_{CC}. So we set up the equation for that particular solution.

$$\left(\frac{2}{3}\right)V_{CC} = \left(\frac{1}{3}\right)V_{CC} + \left(V_{CC} - \left(\frac{1}{3}\right)V_{CC}\right)\left(1 - e^{-\frac{t_1}{\tau_1}}\right) \tag{10}$$

V_{CC} cancels and after combining terms we have

$$\frac{1}{2} = e^{-\frac{t_1}{\tau_1}} \tag{11}$$

We now can solve for t_1.

$$t_1 = \tau_1 \ln(2) \tag{12}$$

$$t_1 = (R_1 + R_2)C \ln(2) \tag{13}$$

For the discharge case

$$V_{C(t)} = \left(\frac{2}{3}\right) V_{CC} e^{-\frac{t}{\tau_2}} \tag{14}$$

We are interesting in the time, t_2, it takes to discharge the capacitor from $(2/3)V_{CC}$ to $(1/3)V_{CC}$.

$$\left(\frac{1}{3}\right) V_{CC} = \left(\frac{2}{3}\right) V_{CC} e^{-\frac{t_2}{\tau_2}} \tag{15}$$

V_{CC} cancels and we have

$$\frac{1}{2} = e^{-\frac{t_2}{\tau_2}} \tag{16}$$

Solving for t_2 gives

$$t_2 = \tau_2 \ln(2) \tag{17}$$

$$t_2 = R_2 C \ln(2) \tag{18}$$

The frequency of oscillation in Hz is

$$F = \frac{1}{t_1 + t_2} = \frac{1}{(R_1 + R_2) C \ln(2) + R_2 C \ln(2)} \tag{19}$$

Simplifying and noting that 1/ln(2) = 1.44 we can now complete the equation for the frequency of oscillation.

$$\boxed{\boldsymbol{F = \frac{1.44}{(R_1 + 2R_2)C}}} \tag{20}$$

Duty-cycle is defined as the time a periodic logic signal is at the '1' state divided by the total period time. Duty-cycle can be expressed as a fraction or in percent. The math that follows will use the fractional form as that is the most direct, particularly for the design equations. All we have to do is combine Equations 13 and 18.

$$D = \frac{t_1}{t_1 + t_2} = \frac{(R_1 + R_2) C \ln(2)}{(R_1 + R_2) C \ln(2) + R_2 C \ln(2)} = \frac{(R_1 + R_2)}{(R_1 + 2R_2)} \tag{21}$$

D can also be expressed in resistor ratio form.

$$\boxed{D = \frac{\left(\frac{R_1}{R_2}\right) + 1}{\left(\frac{R_1}{R_2}\right) + 2}} \quad \textbf{(22)}$$

Design of LM555 oscillator

For design we want the 555 timer to oscillate at a given frequency, F, with a specific duty-cycle, D. D must be greater than 0.5 and less than 1.0.

An analysis of the data sheet results in the following suggested component values for a given desired frequency.

If the frequency of oscillation is between around 1 Hz and around 100 kHz then select a convenient capacitor rounded up or down (perhaps by a factor as much as 3) as needed from the following equation.

$$C_{nominal} = \frac{316\ nF \cdot \sqrt{Hz}}{\sqrt{Frequency\ in\ Hz}} \quad \textbf{(23a)}$$

Generally, R_1 or R_2 should not be much less than around 1,000 ohms or sink currents into pin 7 will become high at first causing frequency errors and damage if severe. Also, it is best that either resistor is not much more than around 1,000,000 ohms so that bias currents of the LM555 do not lead to significant timing errors. If accurate timing is not required then values up to around 10 million ohms can be used particularly if V_{CC} is well above 5 volts. The practical constraints on the resistors leads to practical constraints on the capacitor as described next.

If the frequency of oscillation is less than around 1 Hz then select a convenient capacitor rounded up or down (perhaps by a factor as much as 3) as needed from the following equation.

$$C_{nominal} = \frac{316\ nF \cdot Hz}{Frequency\ in\ Hz} \quad \textbf{(23b)}$$

With the appropriate rounding using one of the above equations we now have a standard value for C. We next solve for the resistor values.

Equation 20 can be expressed in resistor ratio form. The ratio form simplifies design calculations.

$$F = \frac{1.44}{R_2\left(\left(\frac{R_1}{R_2}\right) + 2\right)C} \tag{24}$$

We can first solve Equation 22 for (R_1/R_2).

$$\boxed{\left(\frac{\boldsymbol{R_1}}{\boldsymbol{R_2}}\right) = \frac{\boldsymbol{2D - 1}}{\boldsymbol{1 - D}}} \tag{25}$$

Then using that result in Equation 20 we can solve for R_2.

$$\boxed{\boldsymbol{R_2} = \frac{\boldsymbol{1.44}}{\boldsymbol{FC}\left(\left(\frac{\boldsymbol{R_1}}{\boldsymbol{R_2}}\right) + \boldsymbol{2}\right)}} \tag{26}$$

We next solve for R_1.

$$\boxed{\boldsymbol{R_1} = \boldsymbol{R_2}\left(\frac{\boldsymbol{R_1}}{\boldsymbol{R_2}}\right)} \tag{27}$$

The next step is to round the results for R_1 and R_2 to the nearest standard resistor values. If it is a significant amount of rounding then we might repeat the calculations with a different capacitor. Design is often iterative to find the best solution of a variety of possible solutions.

Example: Design an LM555 oscillator with a frequency of 1 kHz and a duty cycle of 0.75.

Solution: We first calculate a nominal capacitance using Equation 23a of 10 nF. Since that happens to be a standard then we will use C = 10 nF. We next calculate (R_1/R_2) using Equation 25 to be 2.00. We calculate R_2 using Equation 26 as 36K. We then calculate R_1 using Equation 27 as 72K. We will round R_1 to 75K and R_2 happens to be a standard value so we will use R_2 = 36K.

Check: Using Equation 20 we calculate the actual frequency to be 980 Hz and using Equation 22 we calculate the actual duty cycle as 0.755.

A typical schematic diagram for a LM555 oscillator is shown in Figure 5.

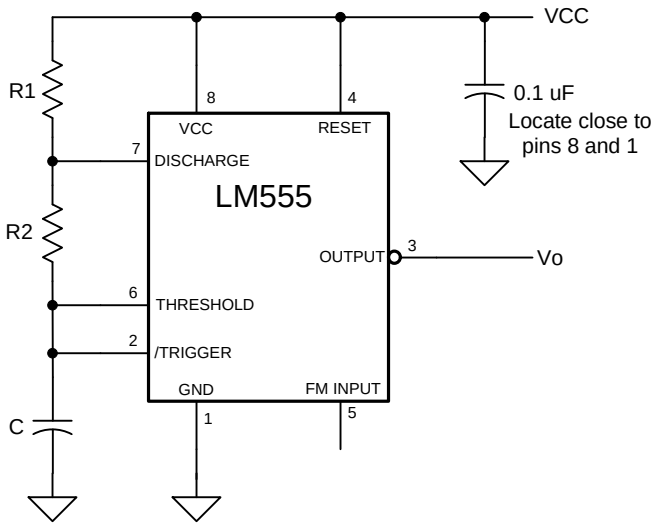

Figure 5: LM555 oscillator circuit

Triangle wave generator

This oscillator is a version of the advanced comparator oscillator that uses a switched constant current source to achieve a linear voltage ramp on the capacitor. It is capable of making very precise voltage ramps. The electronic switch consisting of four diodes routes either the upper current source or the lower current source to the capacitor causing the voltage to rise or fall linearly with time. The unity gain op-amp buffers the voltage across the capacitor and drives the output. The pair of comparators works as in previous circuits to switch the RS flip-flop when the capacitor voltage rises to the upper threshold, V_{UT}, or falls to the lower threshold, V_{LT}. The switch driver is simply a low-impedance buffer driven by the logic from the RS flip-flop and may include some level translation depending on the particular circuit. Figure 6 shows a partial schematic of a constant current charging and discharging type oscillator that produces what is known as triangle waves. Figure 7 shows the voltage waveforms.

Operation of the circuit is as follows. Current sources, I_1, and I_2 are both equal and discussed in the next section. Those currents would typically be a linear function of some applied voltage. Driver, U_1, maps the logic level output of U_6 so that the output high state is higher than V_{UT} and that the output low state is lower than V_{LT}. In some cases this may just be the direct output of U_6.

When the output of U_1 is high then diodes D_1 and D_4 are reverse biased and the capacitor is linearly charged from I_1. Diodes D_2 and D_3 are forward biased. Amplifier, U_2, buffers the voltage across C_1 so that there is “infinite” resistance loading of C_1. When the voltage across the capacitor reaches V_{UT} then the output of comparator, U_3, goes low thus causing the output of U_4 to go high and the output of U_6 to go low.

With the output of U_6 low the output of U_1 is in the low state. D_1 and D_4 are now forward biased and D_2 and D_3 are reverse biased. The current source, I_2, linearly discharges the

capacitor. When the voltage across the capacitor falls to V_{LT} then the output of comparator, U_4, goes low thus causing the output of U_6 to go high and the output of U_5 goes low which latches the state. The oscillation cycle repeats indefinitely.

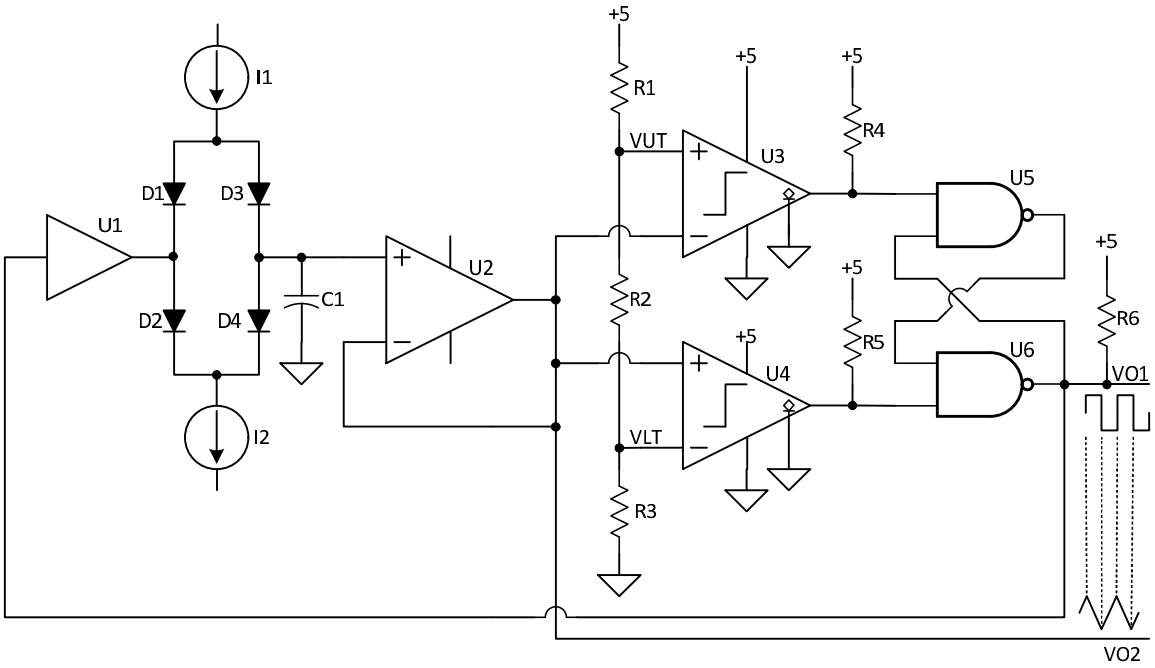

Figure 6: Triangle and square wave generator

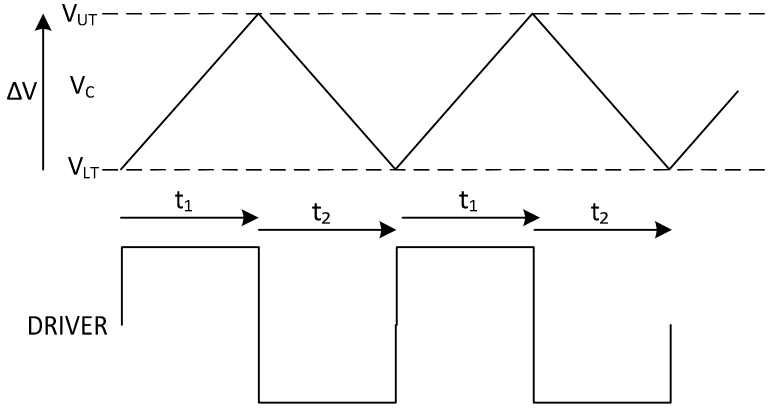

Figure 7: Triangle wave oscillator waveforms

The voltage across a capacitor is the integral of current over time. When a constant current is applied to a capacitor the voltage change per second is constant – thus the straight slopes of the triangle wave.

$$\frac{\Delta V}{\Delta T} = \frac{I}{C} \tag{28}$$

State Machine Oscillators

In the case of the oscillator, ΔV is $V_{UT} - V_{LT}$. The time required for the voltage across the capacitor to change a given ΔV is

$$\Delta T = \frac{C\Delta V}{I} \tag{29}$$

Thus, $t_1$and t_2 are calculated as follows.

$$t_1 = \frac{C\Delta V}{I_1} \tag{30}$$

Note that in the following that I_2 is technically a negative current but ΔV is also a negative value so the minus signs cancel.

$$t_2 = \frac{C\Delta V}{I_2} \tag{31}$$

The frequency of oscillation is calculated as

$$F = \frac{1}{t_1 + t_2} = \frac{1}{\frac{C\Delta V}{I_1} + \frac{C\Delta V}{I_2}} \tag{32}$$

$$\boxed{\boldsymbol{F = \frac{I_1 I_2}{C\Delta V(I_1 + I_2)}}} \tag{33}$$

If the two currents are equal then

$$\boxed{\boldsymbol{F = \frac{I}{2C\Delta V}}} \tag{34}$$

As shown the circuit in Figure 6 with op-amps and standard comparators only works well up to a few tens of kHz or perhaps one hundred kHz or so. For high frequency operation the amplifiers and comparators are replaced with discrete component designs optimized for speed. Such circuits are capable of good performance into the tens of MHz range.

State Machine Oscillators

Voltage Controlled Oscillator

Figure 8 shows a basic voltage to current circuit for a voltage controlled oscillator (VCO) using the circuit in Figure 6. For simplicity a number of refinements are not shown such as proper handling for the case where V_{IN} is less than zero and some feedback management when V_{IN} is very near zero.

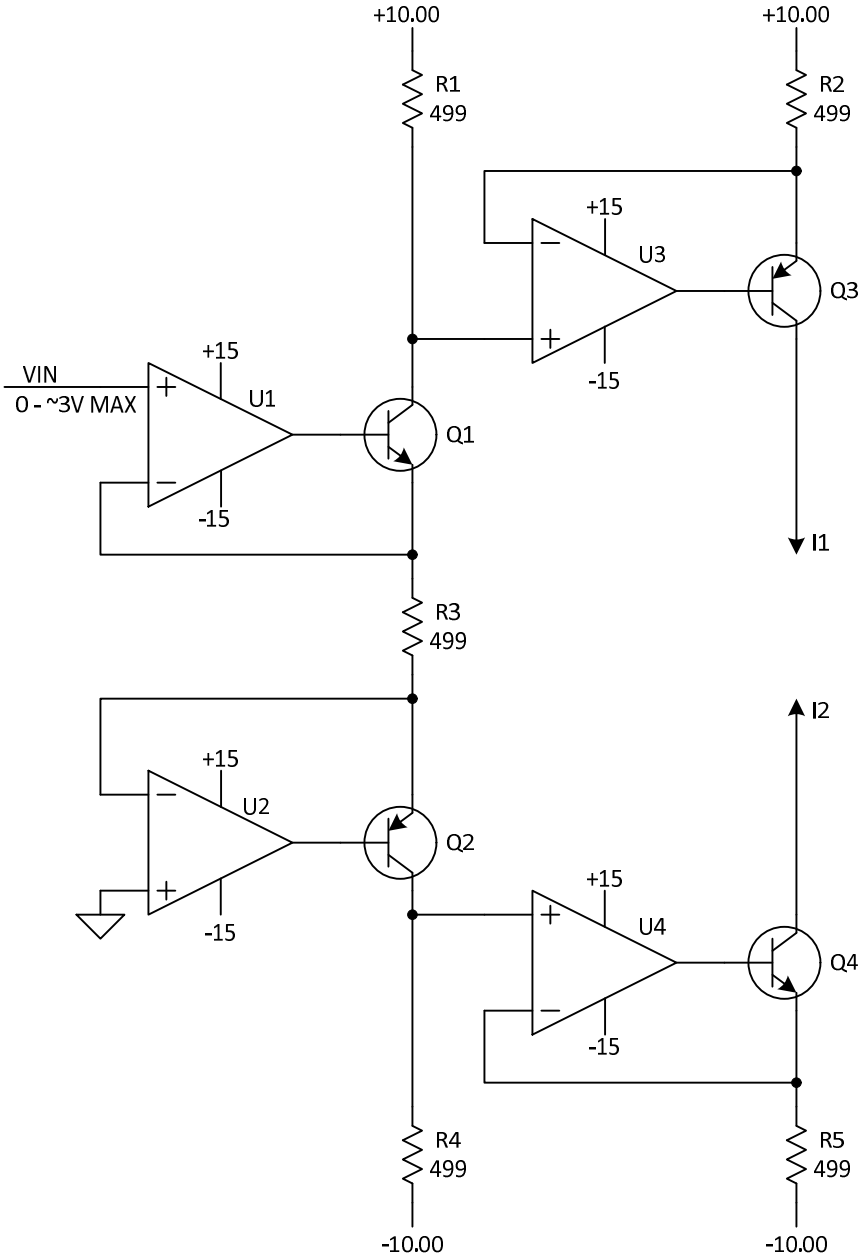

Figure 8: Voltage to current source circuit

Operation of the circuit is as follows. Observe that the inverting input of U_2 is a virtual ground. Next observe that U_1 drives Q_1 so that V_{IN} is across R_3. The emitter current of Q_1 is V_{IN} divided by this resistance. This is also the emitter current of Q_2. For simplicity

we will ignore the small base currents of Q_1 and Q_2. Then the collector currents of Q_1 and Q_2 are the same and directly proportional to V_{IN}. The voltages across R_1 and R_4 are thus both equal to V_{IN}/R_3. U_3 drives Q_3 so that the voltage across R_2 matches that across R_1. Likewise, U_4 drives Q_4 so that the voltage across R_5 matches that across R_4. Thus, the collector currents of Q_3 and Q_4 are identical and equal to V_{IN}/R_3. These would be the current sources for I_1 and I_2 in Figure 6. If constructed with fractional millivolt offset voltage and negligible bias current amplifiers this circuit is capable of linearly converting a voltage to a frequency over a range exceeding three decades. As an example the circuit could be scaled so that a 0 to 2 volt input produced an output frequency 0 to 20 kHz with fairly accurate operation down to below 20 Hz.

All resistors should be matched as close as practical. The 499 ohm value shown is about as small a resistance would be used in an application so that the maximum current through the transistors is less than about 10 mA. To keep the integrating capacitor in Figure 6 a practical value the current has to be relatively high for high frequencies and relatively low for low frequencies. Depending on the needed current to achieve a certain frequency with a practical size capacitor the resistances might need to be larger than 10K. This type of circuit was common in analog function generators of the past and the capacitor was switched by factors of 10 to achieve the different frequency ranges.

The circuit in Figure 9 is an extension of the circuit in Figure 8 that permits the duty cycle of the waveform to be varied with theoretically zero effect on frequency. In practice there will be a small effect on frequency as duty cycle is adjusted – nothing is ever perfect. Operation of the circuit is identical to the previous circuit except that U_1 inverts V_{IN} and there is a potentiometer for adjusting the duty cycle. The currents through R_3 and R_8 are varied depending on the position of the duty cycle control potentiometer, R_6.

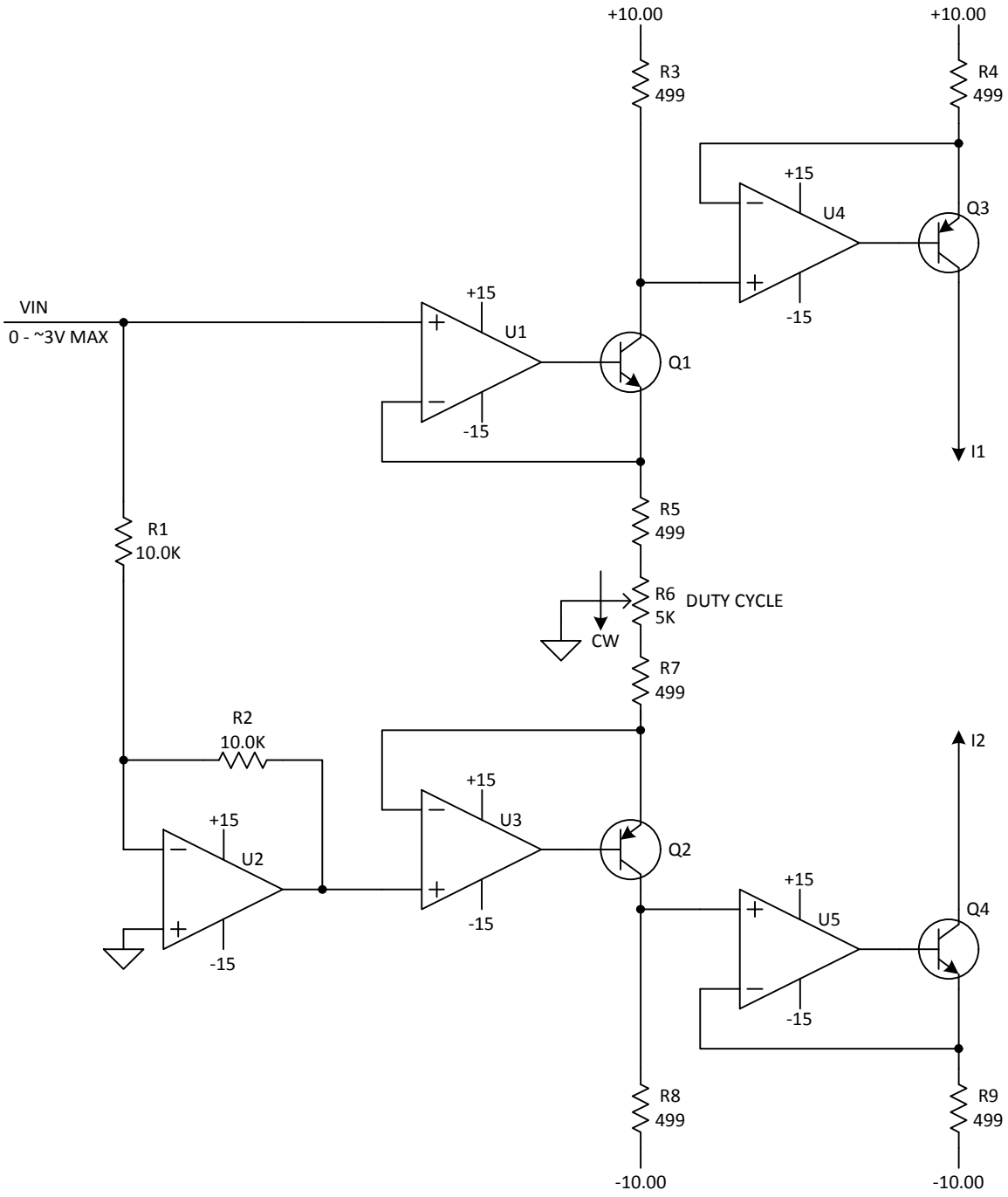

Figure 9: Voltage controlled current sources for variable duty cycle

For simplicity we treat the sum of R_5, R_6, and R_7 as a single resistance, R_T.

$$R_T = R_5 + R_6 + R_7 \tag{35}$$

Then we define a *k* that is a function of the position of the wiper of the potentiometer in relation to the total resistance. The extreme range of *k* is 0 to 1which is impractical. A

different circuit is needed to achieve those extremes. R_5 and R_7 limit the range to be practical. R_5 and R_7 are equal and no smaller than would cause the voltage across either Q_1 or Q_2 to be less than 2 volts at V_{IN} max with R6 at either extreme position. It is not practical with this circuit for the duty cycle to become much less than 0.1 or much greater than 0.9. As shown the range of duty cycle is 0.083 to 0.917 – sufficient for many applications.

$$k = \frac{R_5 + R_{6upper}}{R_T} \tag{36}$$

Because R_4 is equal to R_3 we can write that the current, I_1, is the input voltage divided by the resistance from the emitter of Q_1 to the wiper of the potentiometer which is at ground.

$$I_1 = \frac{V_{IN}}{kR_T} \tag{37}$$

Because R_9 is equal to R_8 we can write that the current, I_2, is the input voltage divided by the resistance from the emitter of Q_2 to the wiper of the potentiometer which is at ground.

$$I_2 = \frac{V_{IN}}{(1-k)R_T} \tag{38}$$

The charging time, t_1, is

$$t_1 = \frac{C\Delta V}{I_1} = \frac{kR_T C\Delta V}{V_{IN}} \tag{39}$$

The discharge time, t_2, is

$$t_2 = \frac{C\Delta V}{I_2} = \frac{(1-k)R_T C\Delta V}{V_{IN}} \tag{40}$$

The frequency of oscillation is

$$F = \frac{1}{t_1 + t_2} = \frac{V_{IN}}{[k + (1-k)]R_T C\Delta V} \tag{41}$$

We note that *k* cancels thus proving that the frequency is independent of the duty cycle.

$$\boxed{\boldsymbol{F = \frac{V_{IN}}{R_T C \Delta V}}} \tag{42}$$

The duty cycle is derived as follows.

$$D = \frac{t_1}{t_1 + t_2} = \frac{\frac{kR_T C \Delta V}{V_{IN}}}{\frac{kR_T C \Delta V}{V_{IN}} + \frac{(1-k)R_T C \Delta V}{V_{IN}}} = k \tag{43}$$

$$\boxed{\boldsymbol{D = k}} \tag{44}$$

The circuit in Figure 9 has the disadvantage that there is DC current through the wiper of the potentiometer. This causes early failure for conventional carbon or various conductive plastic types of potentiometers. A wire-wound potentiometer would be better suited. Another approach is to determine a topology that does not require current through the wiper. That is left as a challenge for the student. The starting point for advanced circuits is simple circuits like this one.